# AN IMPLANTABLE MULTICHANNEL DIGITAL NEURAL RECORDING SYSTEM FOR A MICROMACHINED SIEVE ELECTRODE

T. Akin*, K. Najafi, and R.M. Bradley

*Center for Integrated Sensors and Circuits*
EECS Department, University of Michigan
Ann Arbor, Michigan 48109-2122
* Middle East Technical University, Dept. of Electrical & Electronics Engineering, Ankara, TR-06531, Turkey

## SUMMARY

This paper reports the development of an implantable, fully integrated, single-chip, multichannel neural recording system, which is powered and communicated with using an RF telemetry link. The system allows recording of ±500μV neural signals from axons regenerated through a micromachined silicon sieve electrode. These signals are amplified using on-chip 100Hz to 3.1kHz bandlimited amplifiers, multiplexed, and digitized with a low-power, high speed current-mode 8-bit ADC, and then transmitted out using a passive RF telemetry link. The overall system dissipates 90mW of power from a 5V supply, and occupies 4x4mm$^2$ of area.

## INTRODUCTION

Multichannel recording of neural activity from the central and peripheral nervous systems has long been pursued by physiologists as a means to understand the operation of individual neurons, to decipher the organization and signal processing techniques of biological neural networks, and to control a variety of prosthetic devices. Silicon micromachining and integrated circuit fabrication techniques have been used recently to produce recording probes needed to interface with the nervous system using percutaneous connectors for power and data transfer [1]. However, for many future chronic neural recording applications there is a need for a small, leadless, low-power implantable system with on-chip digitization capability.

Over the past few years, we have been developing a totally implantable neural recording system to be used for multichannel chronic neural recording from individual axons and fibers in the Peripheral Nervous System (PNS) utilizing the nerve regeneration principle of the PNS. We have previously reported on the fabrication and development of a micromachined passive silicon sieve electrode [2]. In addition we have reported the development of an efficient transmitter to transmit sufficient power to small implanted coils [3]. This paper presents the development of a telemetrically powered and controlled digital neural recording system with the necessary on-chip analog and digital circuitry to be used in chronic recording applications. This system is the first of its kind for neurophysiological applications that uses a single monolithic chip which combines signal amplification and filtering, low-power A/D conversion, bi-directional user interface, and RF telemetry units for power/data transfer.

## SYSTEM OVERVIEW

Figure 1 shows the application and structure of the "sieve" electrode recording system. It consists of a micromachined silicon nerve regeneration electrode, a silicon interconnecting cable, on-chip signal processing and telemetry interface circuitry, an RF telemetry link, and an external transmitter. The silicon sieve electrode

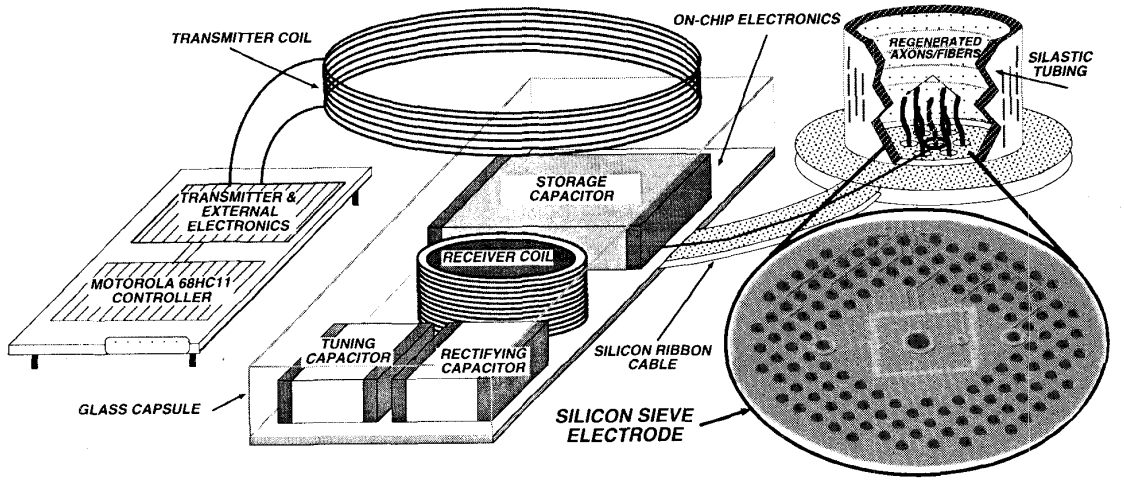



Figure 1: System architecture of a digital neural recording system and structure of a sieve nerve regeneration electrode.

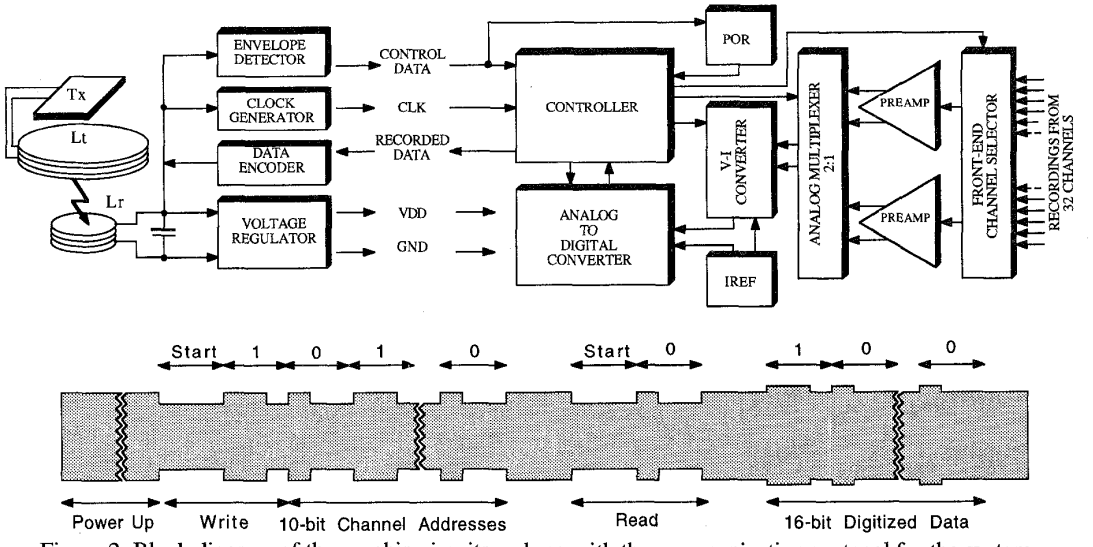



Figure 2: Block diagram of the on-chip circuitry, along with the communication protocol for the system.

supports a large number of small (several microns in diameter) through-holes which allow individual axons of a deliberately severed nerve to regenerate when fixed to the two sides of the electrode. An SEM view of a sieve electrode is also shown in Fig. 1. The recording sites located around through-holes are connected to the signal processing circuitry using a 4μm-thick flexible multi-lead silicon ribbon cable, which is fabricated together with the electrode. Any 2-of-32 recording sites can be selected by a user through address switches at the external controller. A Motorola 68HC11 microcontroller generates serial data to modulate the high-efficiency Class-E transmitter amplifier, which drives a circular transmitter coil. The magnetic field set up by the transmitter coil induces an AC voltage across a receiver coil in the implanted unit. The AM modulated RF signal is used to generate the DC voltage and control data information necessary for the on-chip electronics. Once the chip is programmed, signals from two channels are amplified, time-multiplexed, digitized using a low-power ADC, and transmitted to the outside world using passive RF telemetry.

Figure 2 shows the block diagram of the on-chip circuitry along with the communication protocol for the system. The communication protocol supports two modes of operation: write address and read data. The serial digital signals 1 and 0 are encoded by long and short pulse durations, respectively. Following the start signal, a write command (digital 1) is sent, followed by the 10-bit address (5 bits per channel) of the 2 channels to be selected. Once the channel selection information is transmitted to the on-chip electronics, it waits for the read command (digital 0) to start analog-to-digital conversion of the two channels consecutively and transmits back a total of 16 data bits (8-bits per channel). Then, the on-chip circuitry waits for the next command, and depending on the mode, it either selects the new channels to be recorded from or starts another conversion and transmission cycle. This protocol allows easy synchronization, gives the user control over sampling rate, and is compatible with our RF telemetry system that uses AM modulation and passive reverse telemetry for bi-directional signal transmission.

The implementation of the RF telemetry interface and mixed-mode signal processing electronics is achieved using a BiCMOS fabrication process [4]. In addition to the standard CMOS devices, this technology provides high performance, junction-isolated vertical bipolar transistors and a variety of junction and Zener diodes.

## *CIRCUIT DESCRIPTION*

The three major circuit blocks of the unit are: 1) the voltage regulator; 2) the envelop detector; 3) the preamplifiers; and 4) the analog-digital converter.

***Voltage Regulator:*** The 5-V supply voltage necessary for the implanted electronics is generated by the voltage regulator circuit shown in Fig. 3. The RF signal induced across the receiver coil, which is about 20-V peak, is first rectified by the full-wave rectifier using diodes D1-D8. Good voltage regulation is achieved by setting a constant current in diodes D16-25 through transistors M8, M9 and diodes D13-15. Darlington transistors Q1 and Q2 supply the current to the circuit. Transistors M10-13 and diodes D26-29 keep the voltage regulated against load current variations. In order to improve voltage regulation (necessary for the accuracy of the ADC) and to save lateral area of the implantable unit, capacitors C1, C2, and C3 are chosen to be hybrid capacitors. Simulation and measured results show that the maximum peak-to-peak ripple on top of 5V supply is <0.02V (better than 8 bits). This regulation is maintained during the loading of the receiver coil for reverse passive telemetry using the circuit made of transistors M1-7 and diodes D9-12.

***Envelop Detector:*** A new current-mode envelope detector, shown in Figure 4(a), has been designed to prevent problems associated with the implementation of a conventional detector in CMOS technology. In this circuit, the current through transistors M1 and M5 is different under transient conditions due to different capacitor values for C1 and C2. Therefore, any amplitude change in the RF signal (Vrf) will result in a change in currents through M1 and M5, which are mirrored to M4 and M6, so that they can be compared. Transistors M7 and M8 are used to generate hysteresis to prevent any state change due to ripples on the currents. The detector occupies an area of 0.5 $mm^2$ and consumes a power of only 2 mW. Figure 4(b) also shows the circuit used for extracting the clock signal from the RF carrier.

***Preamplifiers:*** ±500μV neural signals are amplified with two preamplifiers as shown in Fig. 5. Each preamplifier has an in-band AC gain of 40dB with a 3dB bandwidth of 100Hz to 3.1kHz. A special feature of the preamplifier is that it has a DC gain of -40 dB which is

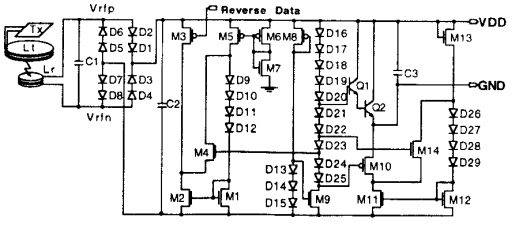
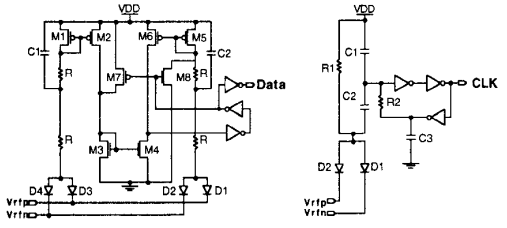



Figure 3: The voltage regulator for the 5V supply shown with the circuitry used for reverse passive telemetry.




(a) (b)

Figure 4: The current-mode envelop detector.

critical in preventing amplifier saturation due to input offset and DC drift caused by the electrode-electrolyte

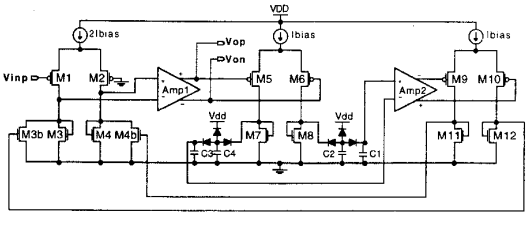



Figure 5: A simplified schematic of the preamplifier.

half-cell. The low cutoff frequency required for DC suppression is achieved using a diode-capacitor filter which prevents the use of chopping or off-chip hybrid components [1], and allows the preamplifier to accommodate a ±500μV signal superimposed on ±160mV DC or low frequency noise. Each amplifier dissipates 0.3mW, occupies 0.2$mm^2$, generates the differential signal for the voltage-to-current converter, and incorporates feedback to prevent output saturation even in the face of very gross process variations.

***Analog-to-Digital Converter:*** A current-mode algorithmic AD conversion approach [5] is used for data conversion, as shown in Fig. 6. Conversion is achieved algorithmically by multiplying the input current (Iin) by two and then comparing it with the reference current (Iref). If 2Iin is larger than Iref then the bit output is "1" and the current, 2Iin-Iref, is fed to the circuit to determine the next bit. Otherwise the bit output is "0", and 2Iin is fed into the circuit to determine the next bit. This continues until the required bits are achieved. The reference current is set at 102.4μA, i.e., a maximum current of only 204.8μA circulates in the circuit at a time. The converter combines the amplifier and the current comparator circuitry and consumes only 2mW, while achieving a conversion accuracy of better than 8 bits with a conversion time of 8μsec per bit. The analog portion of the converter occupies only 0.13$mm^2$, while the digital portion occupies 1.1$mm^2$ in a 3μm CMOS process.

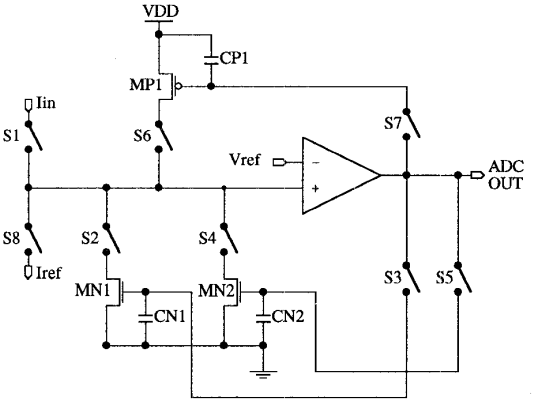



Figure 6: The current-mode algorithmic analog-to-digital converter.

## *TEST RESULTS AND CONCLUSIONS*

The full functionality of the on-chip circuitry has been verified. The fabricated chip, shown in Figure 7, measures 4x6$mm^2$, contains more than 5000 transistors, and dissipates ~90mW of power. The majority (80mW) of this power is consumed by the 5V voltage regulator that provides better than 99.8% regulation. Figure 8 shows a ±400μV signal fed into the preamplifier and the digitized output signal recovered by the external electronics. The voltage signal is amplified, multiplexed, and converted to a current signal, and is then passed

through the analog-digital converter before transmission to the outside world. Figure 9 shows the received RF signal (top trace) which has "read data" command modulated on it, and two 8-bit outputs coming from the ADC (bottom trace), verifying that the on-chip circuitry can be telemetrically powered and controlled. Figure 10 shows a complete sieve electrode telemetry recording system next to a Penny. Note the electrode is connected to the electronics using a silicon ribbon cable, which carries the 32 signals from the recording sites. The size of the total implantable unit, including 3 hybrid capacitors and the receiver coil, measures 5x8x2mm$^3$. An IC chip without the capacitors and coil is also shown.

The entire electronics and components are protected by a glass capsule, with the ribbon cable providing access to the sites. The system has not been tested *in-vivo* yet, and is being prepared for animal implantation.

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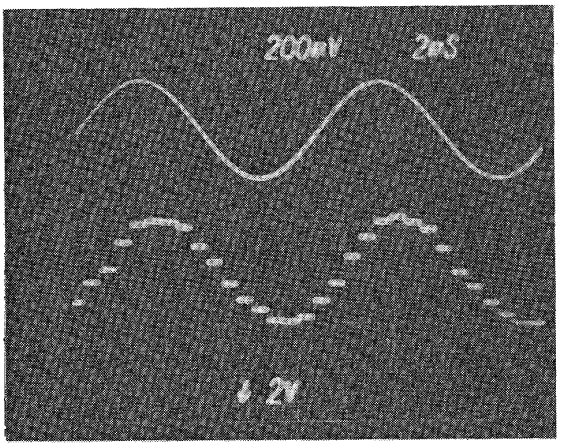



Figure 8: The input to the preamplifier (top trace, a ±400μV sinusoidal signal), and the output digitized signal recovered by the external electronics.

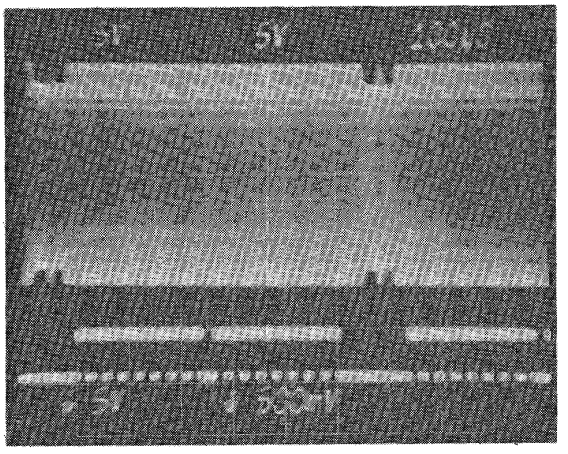


Figure 9: The received RF signal modulated with the "read-data" command, and two 8-bit outputs from ADC.

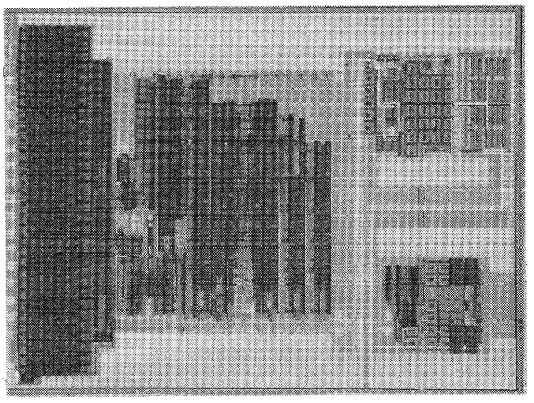


Figure 7: Photograph of the chip fabricated using a 3μm, p-well 1M/2P BiCMOS process.

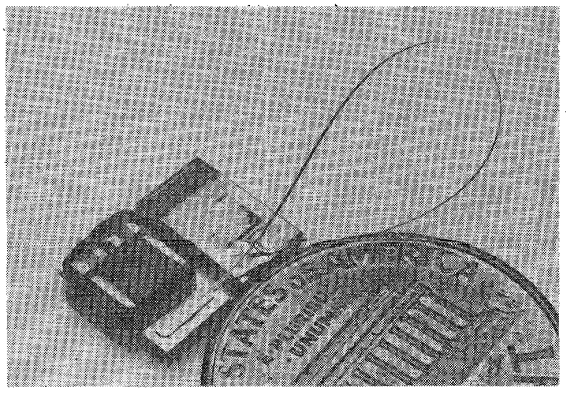


Figure 10: Photograph of a complete sieve electrode telemetry module with silicon cable interconnects.