DESIGN AND OPTIMIZATION OF DIE ON PRINTED CIRCUIT BOARD FOR E-BAND LOW NOISE AMPLIFIERS

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

FARUK KAPLAN

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

DECEMBER 2024

Approval of the thesis:

DESIGN AND OPTIMIZATION OF DIE ON PRINTED CIRCUIT BOARD FOR E-BAND LOW NOISE AMPLIFIERS

submitted by **FARUK KAPLAN** in partial fulfillment of the requirements for the degree of **Master of Science in Electrical and Electronics Engineering Department, Middle East Technical University** by,

Prof. Dr. Naci Emre Altun
Dean, Graduate School of **Natural and Applied Sciences** _____

Prof. Dr. İlkay Ulusoy
Head of Department, **Electrical and Electronics Engineering** _____

Assist. Prof. Dr. Ahmet Cemal Durgun
Supervisor, _____

Examining Committee Members:

Prof. Dr. Seyit Sencer Koç
Electrical Electronics Engineering, METU _____

Assist. Prof. Dr. Ahmet Cemal Durgun
Electrical Electronics Engineering, METU _____

Prof. Dr. Mevlüde Gülbin Dural Ünver
Electrical Electronics Engineering, METU _____

Prof. Dr. Özlem Özgün
Electrical Electronics Engineering, Hacettepe University _____

Assoc. Prof. Dr. Lale Alatan
Electrical Electronics Engineering, METU _____

Date:02.12.2024

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Surname: Faruk Kaplan

Signature :

ABSTRACT

DESIGN AND OPTIMIZATION OF DIE ON PRINTED CIRCUIT BOARD FOR E-BAND LOW NOISE AMPLIFIERS

Kaplan, Faruk
M.S., Department of Electrical and Electronics Engineering
Supervisor: Assist. Prof. Dr. Ahmet Cemal Durgun

December 2024, 89 pages

This thesis focuses on the optimization of die-on printed circuit board (PCB) design for low noise amplifiers (LNA) operating in the extremely high frequency (EHF) band. This frequency band improves the range resolution and accuracy, helping to distinguish near objects. Collision sensors in automotive applications and incoming missile identification systems in military applications utilize the EHF band. The thesis investigates various techniques to enhance performance metrics, such as noise figure (NF) and scattering (S) parameters. The methodology covers a comprehensive literature survey, analytical derivations, and computer simulations using Ansys High-Frequency Structure Simulator (HFSS). Microstrip and coplanar lines, via distribution, wire bond parameters, and compensation configurations, are explored with the aid of HFSS. The thesis hypothesizes that optimizing wire bonds and distributed matching improves S parameters and NF. Also, the mismatch is compensated with capacitive and inductive sections. A hybrid model employing W-elements with discontinuity and mutual capacitance models is studied to decrease the simulation time for matching. After achieving sufficient overlap between the two models, the length and width of matching sections are optimized by using Particle Swarm Optimization

(PSO) for different numbers of stages. Simultaneously, experimental validation is conducted through the manufacturing of test PCBs using a network analyzer tool. In conclusion, this research examines die-on-PCB design optimization for E-band LNAs, incorporating methodological perspectives. The findings have implications for the development of EHF systems and contribute to the field of RF engineering.

Keywords: Extremely high band, Low noise amplifier, Scattering parameter, Compensation circuit, Particle swarm optimization

ÖZ

E-BANT DÜŞÜK GÜRÜLTÜLÜ YÜKSELTEÇLER İÇİN BASKI DEVRE KARTI ÜZERİ YONGA TASARIMI VE EN UYGUNLANMASI

Kaplan, Faruk
Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü
Tez Yöneticisi: Dr. Öğr. Üyesi. Ahmet Cemal Durgun

Aralık 2024 , 89 sayfa

Bu tez, son derece yüksek frekans (EHF) bant aralığında çalışan düşük gürültülü yükselteçler (LNA) için baskı devre kartı (PCB) tasarımının optimizasyonuna odaklanmaktadır. Bu yüksek frekans menzil çözünürlüğü ve doğruluğunda iyileştirmelerle, yaklaşan nesneleri ayırt etmeye yardımcı olmaktadır. Çarpışma sensörü gibi otomotiv uygulamalarında ve yaklaşan mühimmatın kimliklendirilmesi gibi askeri uygulamalarda EHF bandından faydalanılmaktadır. Ayrıca çalışmada, gürültü figürü (NF) ve saçılma (S) gibi performans parametrelerini iyileştirmek için çeşitli teknikler araştırılmaktadır. Metodoloji, kapsamlı bir kaynak taraması ile başlayıp, analitik türetmeler ve Ansys HFSS kullanılarak simülasyonlar ile devam etmektedir. Mikroşerit ve eş düzlemli hat tipleri, deliklerin dağılımı, tel atlama parametreleri ve eşleme konfigürasyonları incelenmiştir. Hipotez, tel atlamaları ve dağıtık eşlemeyi optimize etmenin S parametrelerini ve NF'yi iyileştireceğini öne sürmektedir. Empedans uyumsuzluğu kapasitif ve endüktif hat parçalarıyla telafi edilmektedir. Benzetim süresini kısaltmak için, süreksizliği ve ortak kapasitif etkiyi de kapsayan bir W-eleman hibrit modeli oluşturulmuştur. 3 boyutlu model sonucu ile yeterli örtüşme sağlandıktan sonra, PSO

algortiması kullanılarak eşleme devresi parçalarının boyutları en uygunlanmıştır. Eşzamanlı olarak, test kartlarının deneysel doğrulamaları bir ağ çözümleyici aracı kullanılarak yapılmıştır. Sonuç olarak, bu araştırma, E-bandındaki yükselteçler için PCB üzeri yonga tasarımı en uygunlamasının kapsamlı bir incelemesini sunmakta ve yöntembilimsel bakış açıları içermektedir. Bulgular, yüksek frekanslı RF sistemlerinin geliştirilmesi için önemli sonuçlar doğurmakta ve RF mikrodalga mühendisliği alanına katkıda bulunmaktadır.

Anahtar Kelimeler: Aşırı yüksek bant, Düşük gürültülü yükselteç, Saçılma parametresi, Eşleme devresi, Parçacık sürü optimizasyonu

"For those who fill my life with inspiration..."

ACKNOWLEDGMENTS

I want to express my gratitude to my supervisor, Assistant Prof. Ahmet Cemal Durgun, for his invaluable guidance and support. His encouragement was instrumental in completing this thesis.

I would also like to extend my heartfelt thanks to the jury chairman, Prof. Seyit Sencer Koç, for his insightful feedback and guidance, as well as to the jury members Prof. Mevlüde Gülbin Dural Ünver, Prof. Özlem Özgün, and Assoc. Prof. Lale Alatan, thank you for your contributions and support during the evaluation process. Your expertise and input have greatly enriched this work.

I am also thankful to my manager, Ahmet Aktuğ, and team leader, Volkan Açıkel, PhD, for their encouragement and assistance throughout this thesis. I am deeply grateful to Mustafa Kaan Çan, who is currently pursuing his PhD degree at Bilkent University, for his support and for teaching me critical aspects of LNA design and die-on PCB modeling. Additionally, I appreciate the help of all prototyping and production line co-workers, including the clean room facility at Aselsan Inc.

A heartfelt thank you to my family and my girlfriend for their unwavering support and encouragement, which gave me the strength to finalize this thesis.

TABLE OF CONTENTS

ABSTRACT v

ÖZ vii

ACKNOWLEDGMENTS x

TABLE OF CONTENTS xi

LIST OF TABLES xiii

LIST OF FIGURES xiv

LIST OF ABBREVIATIONS xix

CHAPTERS

1 INTRODUCTION 1

1.1 Motivation and Problem Definition 1

1.2 Proposed Methods and Models 5

1.3 Contributions and Novelties 11

1.4 The Outline of the Thesis 11

2 LOW NOISE AMPLIFIERS AT EXTREMELY HIGH FREQUENCY BAND 13

2.1 Low Noise Amplifier Essentials 13

2.1.1 Operating Frequency and Fractional BW 13

2.1.2 Noise Figure and Friis Formula 14

2.2 E-BAND PROCESS CHALLENGES 16

2.2.1 PCB Substrate, Finishing, and Manufacturing Limits 17
2.2.2 Interconnection Types, Effects, and Parameters 25
2.2.3 PCB Cavity Limitations 28
3 DESIGN METHODOLOGY 31
3.1 Building Blocks: IC and PCB 31
3.2 Numerical Modeling 33
3.2.1 Port and Transmission Line Definitions 34
3.2.2 Wire-Bond Modelling 40
3.2.3 Compensation Structures: Grooving and Multi-section 45
3.3 Uncompensated LNA PCB Measurements 50
4 MATCHING SECTION DESIGN AND OPTIMIZATION 55
4.1 2D/3D Hybrid Model 55
4.2 Low Fidelity Optimization using PSO Algorithm 68
5 CONCLUSIONS 81
REFERENCES 83
APPENDICES
A PSO ALGORITHM KEY CONCEPTS 89

LIST OF TABLES

TABLES

Table 2.1 Comparison of Dielectric Substrates 18

Table 2.2 Comparison of the IL of Surface Finishes 20

Table 3.1 Comparison of MKR-Tech TeraHertz Chip List 32

Table 4.1 Weak Mutual Capacitance Between Far Sections 66

Table 4.2 Comparison of ILs for Matching Sections 80

Table 4.3 Objective Function Values for Different Cases 80

LIST OF FIGURES

FIGURES

Figure 1.1 Frequency Band Divisions 2

Figure 1.2 Transition from 24 to 77 GHz Frequency Band 3

Figure 1.3 Ultra SRR Image Illustration [3] 3

Figure 1.4 Typical RX Structure 4

Figure 1.5 Typical Amplifier Block Scheme 4

Figure 1.6 Analog Devices HMC8325 Product [9] 6

Figure 1.7 Grooving Method for Bonding 7

Figure 1.8 Adjustable MMIC Capacitance Usage [17] 8

Figure 1.9 Shunt Capacitance and Ground Plane Techniques 8

Figure 1.10 L-C-L, 7-Stage Filter, λ/4 and λ/2 Approaches [19] 9

Figure 1.11 Differential L-C-L and Micro-strip Stub Solutions [20] 9

Figure 1.12 3D Models of Planar and Bond-wire Based Matching 10

Figure 1.13 Compensation Model Dimension Optimization [22] 10

Figure 2.1 The Cascaded System Given By F and G Values 16

Figure 2.2 Flanged Transistor in All-Through Cavity on PCB [29] 17

Figure 2.3 IL at 77 GHz [30] 18

Figure 2.4 SR Analysis 19
Figure 2.5 Nickel and Palladium Plating Models 21
Figure 2.6 IL ($|S_{21}|$) Effect of Ni and Pd 21
Figure 2.7 ENEPIG and Electro-deposited Copper PCB 22
Figure 2.8 S-Parameters of ENEPIG and Electro-deposited Copper PCB . . 22
Figure 2.9 ENIG Finished PCB 23
Figure 2.10 S-Parameters of ENIG Finished PCB 23
Figure 2.11 IG Finished PCB and Results 24
Figure 2.12 CPWG Distributed Matching Limitations 24
Figure 2.13 Wire-Bond Model Side View 25
Figure 2.14 Hot Via Implementation [40] 26
Figure 2.15 3D Model and Results of Bond Diameter 27
Figure 2.16 3D Model and Results of Number of Bonds 28
Figure 2.17 3D Model of Shifting the Die within the Cavity 29
Figure 2.18 Return Loss (S_{11}) Effect of Die Shift in Cavity 29

Figure 3.1 SMM5727XZ Product with WLCSP Technology [41] 32
Figure 3.2 HMC8325 Product Under Microscope 33
Figure 3.3 Intel Benchmark Problem RL and IL 35
Figure 3.4 PCB and Connector Dimension Comparison 36
Figure 3.5 Broadband S-Parameters for Detailed Thru Line Model 36
Figure 3.6 Complete Q2D CPWG Structure 37
Figure 3.7 Effect of Port Dimensions 38

Figure 3.8 RL (S_{11}) Effect of Port Dimensions 39

Figure 3.9 3D Model and Results of Via Staggering 39

Figure 3.10 JEDEC 4 Point Wire-Bond 40

Figure 3.11 Two Different Approaches for Bonds 41

Figure 3.12 RL S_{11} for Different Bond Profiles 41

Figure 3.13 Height and Gap Parameters of the Bond 41

Figure 3.14 Effect of Height and Gap Parameters of the Bond 42

Figure 3.15 Sharp and Smooth Taperings in the Same Length 43

Figure 3.16 RL Effect of Short Width Discontinuity 43

Figure 3.17 RL Effects of Through-Through and Through-Pad Bonding . . . 44

Figure 3.18 RL (S_{11}) Effect of Multi-Bonding 45

Figure 3.19 HMC8325 S Parameters 46

Figure 3.20 Q2D Model for Microstrip Line on Die 46

Figure 3.21 HFSS Initial Model for Die in PCB Cavity 47

Figure 3.22 HFSS Half Model with Die Ports 48

Figure 3.23 Return Loss (S11) Effect of Die Port Definition 48

Figure 3.24 3D Model and Results of Epoxy Height 49

Figure 3.25 Uncompensated PCB Design with Cavity and DC Circuitry . . . 50

Figure 3.26 Ribbon and Wire Bondings Under Microscope 51

Figure 3.27 Measurement Setup 52

Figure 3.28 Signal Analyzer Result 52

Figure 3.29 Measured Gain vs Input Power for the Uncompensated Design . 53

Figure 3.30 Measured Gain vs Frequency for the Uncompensated Design . . 53

Figure 3.31 Measured NF for the Uncompensated Design 54

Figure 4.1 Exemplary 3D Matching Design 56

Figure 4.2 Proposed Hybrid Model for Optimization 56

Figure 4.3 Model Comparison for Through Line 57

Figure 4.4 RL (S11) Effect of W-Element on 5 mm Through line 57

Figure 4.5 Q2D Models of Narrow and Wide Line Sections 58

Figure 4.6 Models for Through and 1 mm Capacitive Lines 58

Figure 4.7 Microstrip Discontinuity of Change in Width 59

Figure 4.8 Updated W-Element Model of Through-Capacitive Lines 59

Figure 4.9 RL (|S_{11}|) Effect of W-Element on 1 mm Capacitive Line 60

Figure 4.10 Asymmetric Matching and Resultant Field 60

Figure 4.11 HFSS Model for Parametrization of C Line Between Ls 61

Figure 4.12 Curve Fitting for Length of C and Discontinuity L Value 62

Figure 4.13 Cascaded W-Element Model of Through and 1 mm Inductive Lines 62

Figure 4.14 Electric Field Plots for C-C and C-L-C Cases 63

Figure 4.15 Mutual Capacitance Values of Consecutive Wide Lines 64

Figure 4.16 Projections of the 3D Surface Result 64

Figure 4.17 RL (|S_{11}|) Effect of W-Element on 1 mm Inductive Line 65

Figure 4.18 Cascaded W-Element Model of 2 Stage LC Lines 65

Figure 4.19 2 Stage LC Lines HFSS and W-Element Compatibility 66

Figure 4.20 Uncompensated Model and Result 67

Figure 4.21 Circuit Representation of Cascaded Wire-bond and Inductance . 68

Figure 4.22 HFSS Model of Wire-bond and Inductance 68

Figure 4.23 Summation of Penalties Representation 70

Figure 4.24 RL (lS_{11}l) Effect of Only Inductive Section 72

Figure 4.25 Complete W-Element Model for 1 Stage LC Matching 72

Figure 4.26 HFSS Model for 1 Stage LC Matching 73

Figure 4.27 RL (lS_{11}l) for 1 Stage LC Matched Bond 74

Figure 4.28 Swarm Behavior of Particles within Iterations 74

Figure 4.29 Complete W-Element Model for 2 Stage LC Matching 75

Figure 4.30 HFSS Model for 2 Stage LC Matching 75

Figure 4.31 RL (lS_{11}l) for 2 Stage LC Matched Bond 76

Figure 4.32 Complete W-Element Model for 3 Stage LC Matching 76

Figure 4.33 HFSS Model for 3 Stage LC Matching 77

Figure 4.34 RL (lS_{11}l) for 3 Stage LC Matched Bond 78

Figure 4.35 Performance Metrics for Varying Number of Stages 79

LIST OF ABBREVIATIONS

2D	Two Dimensional
3D	Three Dimensional
ADC	Analog to Digital Converter
BW	Bandwidth
CPWG	Coplanar Waveguide
DAC	Digital to Analog Converter
DC	Direct Current
EHF	Extremely High Frequency
EM	Electromagnetic
ENIG	Electroless Nickel Immersion Gold
ENEPIG	Electroless Nickel Electroless Palladium Immersion Gold
F	Noise Factor
FFT	Fast Fourier Transform
HFSS	High-Frequency Structure Simulator
IL	Insertion Loss
ISIG	Immersion Silver Immersion Gold
ISM	Industrial, Scientific and Medical
JEDEC	Joint Electron Device Engineering Council
LNA	Low Noise Amplifier
LRR	Long Range Radar
MMIC	Monolithic Microwave Integrated Circuits
NB	Narrow Band
NF	Noise Figure
PCB	Printed Circuit Board

RF	Radio Frequency
RL	Return Loss
RLGC	Resistance Inductance Conductance Capacitance
RX	Receiver
S	Scattering
SHF	Super High Frequency
SNR	Signal to Noise Ratio
SR	Surface Roughness
SRR	Short Range Radar
TL	Transmission Line
UWB	Ultra Wide Band
WLCSP	Wafer Level Chip Size Packaging

CHAPTER 1

INTRODUCTION

1.1 Motivation and Problem Definition

In the realm of science and technology, various advancements across periods have always been fueled by a necessity for answers to tackle changing issues. In the domain of electronics engineering, significant strides have been achieved in essential constraints like operational frequency and the shrinking of devices. These progressions have mainly been facilitated by innovations in material science that have cleared a path for the creation of top-notch radio frequency (RF) and microwave components. The frequency capabilities of these components have seen a rise in the past few decades, which has led to exciting advancements in communication technology as well. One essential feature of electromagnetic (EM) waves is the inverse connection between frequency and dimension. In contemporary semiconductor technology, where transistors have become smaller due to improvements, this idea is essential. Data transmission speeds rise with decreasing transistor sizes, allowing for faster digital-to-analog (DAC) and analog-to-digital (ADC) converters [1]. Moreover, the shift to higher frequencies, which have shorter wavelengths, offers other advantages, including better resolution for detection and range applications. These patterns highlight how frequency, dimension, and performance interact in sophisticated electronic systems.

The very first step of designing these RF systems is choosing the suitable operational frequency band. The mentioned frequency bands vary from 3 Hz to 3 THz as in Figure 1.1, and they are divided into sub-categories according to the International Telecommunication Union. Because of the limitations in manufacturing, most of the

academic and industrial works are done up to super high frequency (SHF), which is below 30 GHz. In the last decades, EHF band microwave component studies have started to be conducted in the literature [2]. From the implementation point of view, two main areas require EHF components: the automotive and defense industries. In the automobile sector, radar applications are divided into two categories: corner radars and front radars. The former one is located at the back and front corners of vehicles and performs short range radar (SRR) duties such as blind-spot recognition. In contrast, the latter one is intended for long range radar (LRR) applications like adaptive cruise control. This radar is also used in industry for fluid-level sensing. In the military sector, sensitive detection of the incoming missile is crucial. The distinct parts of an ammunition system are intended to carry out a particular function, such as explosion, propulsion, or guidance. The operational frequency should be increased to distinguish these parts in a nearby area.

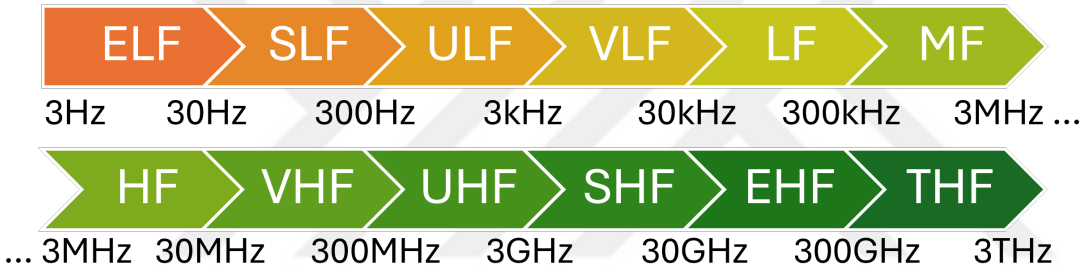


Figure 1.1: Frequency Band Divisions

The primary motivation behind the frequency choice is that the 24 GHz band is being gradually removed for future use. Due to regulatory changes, only the narrow band (NB) industrial, scientific and medical (ISM) band will be accessible. This limitation has resulted in a shift towards the 77 GHz band, as shown in Figure 1.2, which offers a significant advantage due to its broader bandwidth (BW) [3]. In particular, the radar frequency range of 76-81 GHz has a maximum BW of 5 GHz, improving both accuracy and resolution in detecting target distances.

The 77 GHz ultra wide band (UWB) radar with 5 GHz BW offers a range resolution up to 20 times greater than that of the 24 GHz NB radar, which has a BW limit of 250 MHz because range resolution is inversely proportional with the BW. This is crucial for precise measurements and advanced applications in automotive and indus-

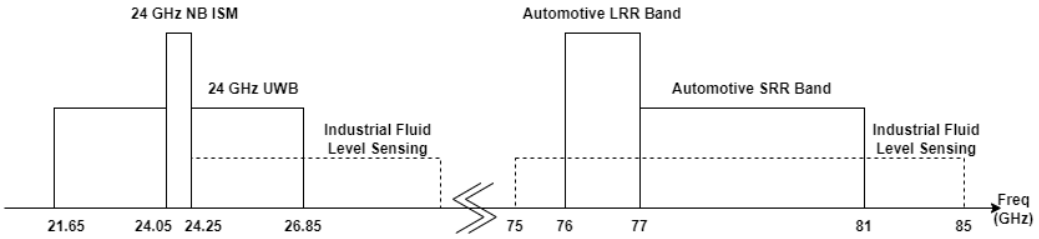


Figure 1.2: Transition from 24 to 77 GHz Frequency Band

trial settings. Additionally, the higher frequency of 77 GHz radar enhances velocity resolution and precision, making it ideal for car park-assist systems requiring precise movements. The velocity resolution is advanced by a factor of 3, assuming observation time T_r is the same, which relies on the fact that velocity resolution is inversely proportional to the frequency. Moreover, sensors can be made smaller due to their higher frequency. This characteristic is beneficial in industrial and automotive settings where a reduced beam width helps minimize interference. These two pieces of information are combined and displayed as a 2-D fast Fourier transform (FFT) range-velocity picture of a point object at 1 m as in Figure 1.3, demonstrating enhanced resolution with 77 GHz. The signal strength is still highest at 1 m in the range direction at 24 GHz, but it is distributed along the interval of 0 to 3.5 m. Similarly, the relative speed is spread between -1 and +1 km/h interspace.

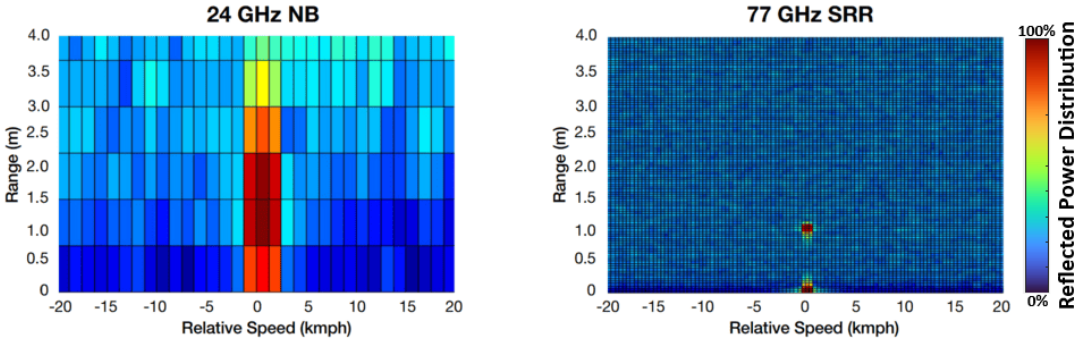


Figure 1.3: Ultra SRR Image Illustration [3]

After choosing the frequency band, one should continue with the system specifications, which leads to the selection of the subsystem component. This encompasses the associated technologies used to transmit, receive and process signals. Each radar system requires a receiver (RX) structure, and a typical one consists of antennas, low

noise amplifiers (LNA), mixers, oscillators, and filters as seen in Figure 1.4. Defining parameters for these systems can be seen as frequency, BW, noise figure (NF), S-parameters, and saturation power [4]. NF is the degradation of the signal to noise ratio (SNR) between the input and output of the device at a constant temperature. Also, the overall NF of a cascaded system is mainly determined by the NF and gain of the first stage. A low NF and high gain indicate better performance, meaning the RX can process weaker signals. Hence, an LNA component is required in this EHF application whose internal structure is given in Figure 1.5.

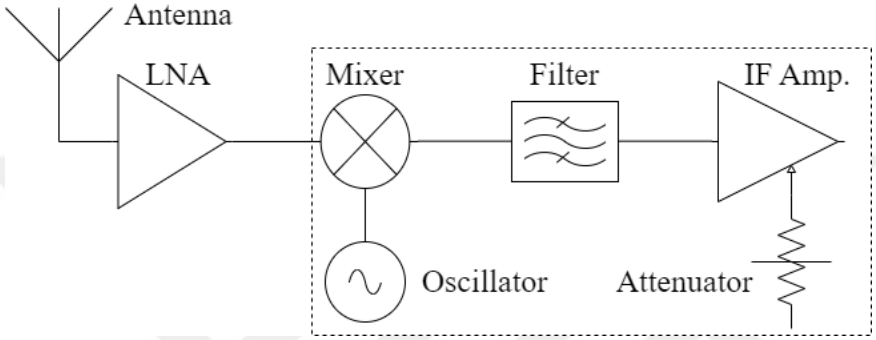


Figure 1.4: Typical RX Structure

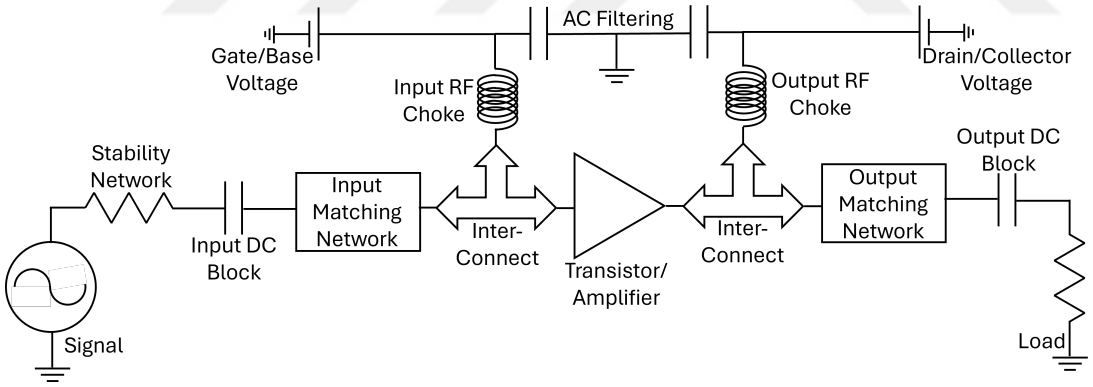


Figure 1.5: Typical Amplifier Block Scheme

Once the necessity of the LNA usage is solidified, the next step is finding a suitable transistor component. Since the TX part of the EHF radar systems is already built on PCB technology, the LNA design must be on the same interface. There are packaged or flip-chip top-shelf components and die components. However, the loss caused by those packages dramatically increases with the frequency [5]. Hence, it is

decided to start with a die transistor, and there are different component opportunities for dies, i.e., monolithic microwave integrated circuits (MMIC). The problem of using a die component on top of the PCB mainly arises from the parasitic effects of the interconnections [6]. This parasitic changes the impedance seen from the input, and the overall S-parameters degrade from the initial die values depending on the chosen bonding technology and geometry. This challenge can be partly recovered by process enhancements such as grooving the die in a PCB cavity and using a shorter, thicker, and flatter interconnection. The remaining deterioration in S-parameters should be compensated by using capacitive and inductive matching sections on the PCB. At the EHF band, optimization of the width and length dimensions of the matching circuit results in significant computational load and extended simulation time.

The main aim of this thesis is to propose a compensation circuit design and optimization using a hybrid model consisting of W-element models and lumped elements. The W-element refers to resistance, inductance, conductance, and capacitance (RLGC) per unit length parameters of transmission line (TL) gathered from Ansys Q2D simulations [7]. This hybrid model is used in a PSO algorithm, and S-parameters are improved. With the help of this new model, the optimal matching circuit is achieved more easily and quickly without sacrificing accuracy.

1.2 Proposed Methods and Models

In this study, a commercial single-chip solution of Texas Instruments is the starting point. AWR2243 is a frequency-modulated continuous wave transceiver with a typical NF of 13 dB at these frequencies [8]. This 13 dB NF value limits the minimum detectable signal level and dynamic range of the RX. It should be cascaded with a low noise and medium gain amplifier to improve the overall NF of the system, which yields an LNA necessity. The suggested LNA approach covers several specific points, starting with finding a die component from ready-to-use options. Analog Devices HMC8325 die product seen in Figure 1.6 is found to be suitable with typical 3.6 dB NF [9]. While interconnections are expected to degrade the NF, the primary objective of this study is to develop a compensation strategy to mitigate these effects.

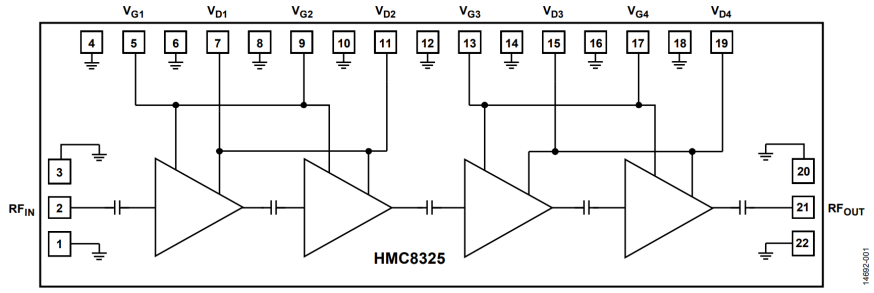


Figure 1.6: Analog Devices HMC8325 Product [9]

The decision process should continue with the proper substrate selection for PCB. Several substrate options are characterized mainly by dielectric constants, loss tangent (dissipation factor), and heights (h). Other side properties are finishing types like gold (Au), silver (Ag), nickel (Ni), palladium (Pd), or their different combinations. These are known as ENIG, ENEPIG, ISIG, etc., where E and I stand for electroless and immersion, respectively. After selecting the proper dielectric substrate, the next stage is determining the interconnection between the PCB and the die.

There are two main processes for this interface, namely wire bond and ribbon. These two different types of interconnections are examined in the literature, and their effects on S-parameters are investigated [10]. There are wire bond modeling studies involving diameter, length, and height sweeps. One of these studies was conducted for die-substrate interconnection, and it used only one wire bond. However, there is a 15 dB RL difference between simulation and de-embedded measurement at SHF band [11]. Another study is conducted for a 10 times shorter bond. The simulation and experimental results are similar with a 1 dB RL difference at K-band [12]. These are the baselines to ensure the bond characteristics. The ribbon usage enhances the signal performance, which is shown by a comparative study [13]. It has an enhancement of 1 dB insertion loss (IL) at K_u band for the same pad width, height, and distance as the wire ball bonding. Another research uses ribbon bonding, and it achieves very low IL at the W-band in the measurement [14].

Up to this point, it is assumed to make a bonding between two TLs or die on top of the PCB. However, placing the die on the surface creates a height difference between bonding pads. In addition, there is a minimum height limit for the bond to be bent, depending on the process. The summation of these two height values makes the inter-

connection longer, and the IL and inductance rapidly increase, especially in the EHF band. Hence, the die component should be grooved into a cavity that is sensitively opened in the PCB, as shown in Figure 1.7. There are a limited number of investigations in the literature, and the term grooving is also mentioned as an embedded die or cavity down. One of these studies involves a recessed cavity for mounting an MMIC RF amplifier and mixer [15]. These chips are fixed with epoxy on an alumina substrate, and interconnections are realized by wire bonds and multiple bonds, while ribbons are suggested in future work. The measured performance parameters are given for the overall substrate-integrated waveguide (SIW) design, which has a high IL at V-band.

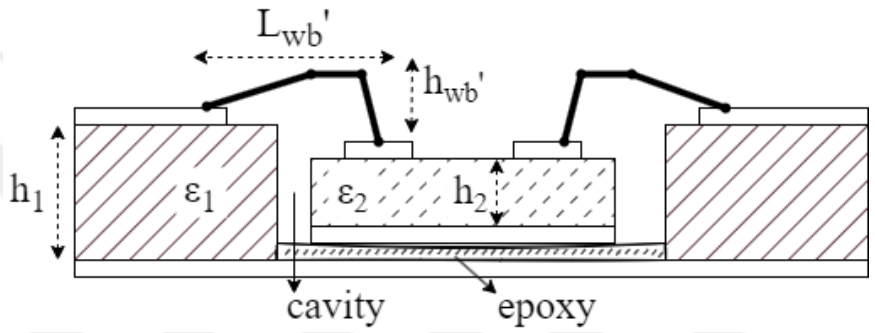


Figure 1.7: Grooving Method for Bonding

Combining all previous process information, such as PCB and interconnection properties, there are multiple reflections to be compensated. Hence, the interconnection should be followed by lumped and distributed circuit components for biasing and matching sections [16]. Since all types of interconnections add impedance discontinuities, there is a need for specific matching circuits that transform this reactive impedance to tolerable values. In the literature, there are applied compensation structures, and one of them proposes on-chip capacitance [17]. These capacitors given in Figure 1.8 can be seen as static or dynamic compensators whose values are adjustable. Yet, this implementation needs direct involvement in the MMIC design process, and top-shelf die components cannot be adapted to this wafer process.

One of the other examinations relies on only the usage of lumped and distributed capacitances on PCB [18]. Two different approaches are applied, and one of them is the usage of lumped elements at the beginning and end points. The other method uses

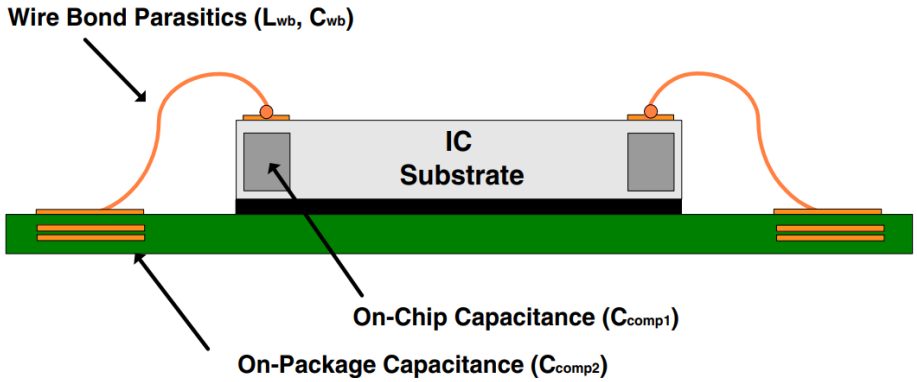


Figure 1.8: Adjustable MMIC Capacitance Usage [17]

a via embedded ground plane under the wire bond gap as shown in Figure 1.9. After parametrization of the capacitance values and ground plane dimensions, the structure results in -20 dB RL and -6 dB IL at 17 GHz. However, lumped element usage is not applicable to the EHF band, and the ground plane under the bond requires equal height and no vertical gap between the input and output lines.

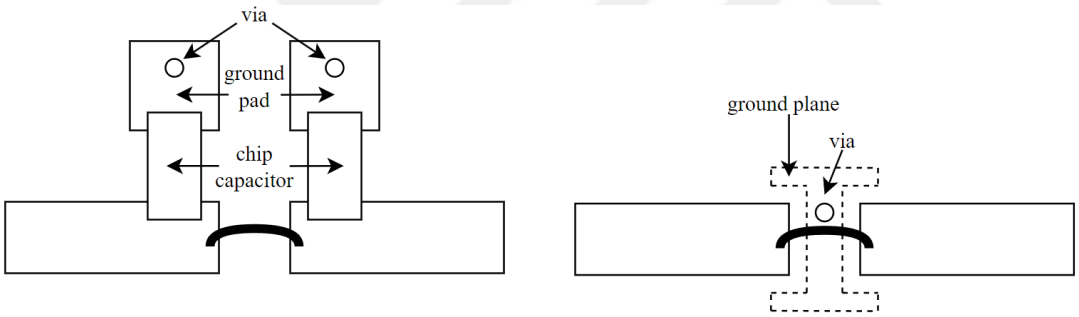


Figure 1.9: Shunt Capacitance and Ground Plane Techniques

Another study compares different types of compensation circuits, including L-C-L low pass, seven-stage filter, $\lambda/4$ length transformer, and $\lambda/2$ line with additional PCB section as shown in Figure 1.10. The first one is useful only for lower frequencies, while the multistage filter can provide band-pass characteristics for planar applications. The $\lambda/4$ method is more straightforward to realize, but it has a very narrow BW and low robustness against tolerances. The $\lambda/2$ approach has a relatively wider band, but it increases the IL significantly [19]. All of these proposed solutions are conducted in schematic and layout phases, and the 3-D results do not overlap with the expectations.

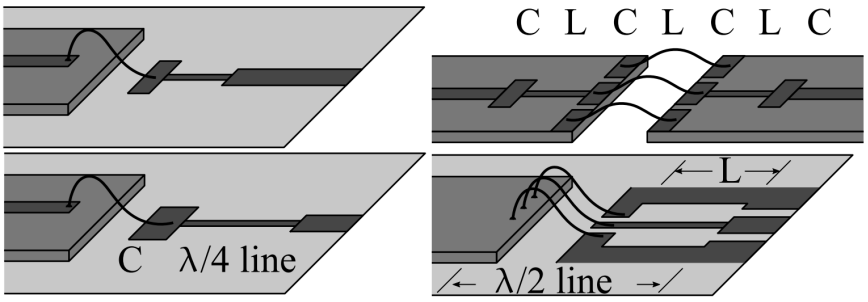


Figure 1.10: L-C-L, 7-Stage Filter, $\lambda/4$ and $\lambda/2$ Approaches [19]

Yet another research focuses on the interconnection between TX/RX antennas and the chip-set, which includes a mixer [20]. It suggests two different methods, namely differential L-C-L and micro-strip stubs, as shown in Figure 1.11. In both of the methods, the notch frequency changes dramatically depending on the practical length of the wire bond. Apart from the manufacturing dependency, the dimensions of the distributed elements are optimized in 3-D for a single time, and the design must be done from scratch in every iteration.

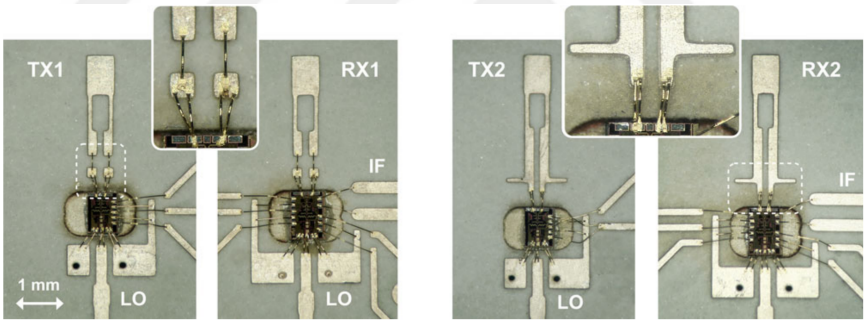
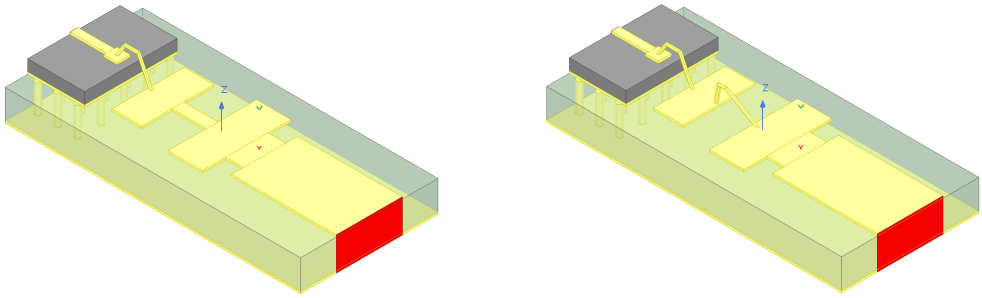


Figure 1.11: Differential L-C-L and Micro-strip Stub Solutions [20]

When the required matching inductance value gets higher, the width of the matching section gets narrower and is limited by the PCB production. In order to overcome this problem, there are proposed ways where this inductance is realized by another wire-bond connection [21]. The three dimensional (3D) recommended models seen in Figure 1.12 are re-created within the simulation environment, but the same result does not emerge.

The last study combines the compensation structure and optimization algorithm [22]. The substrate, the chip, two signal bonds, and two ground bonds are modeled in



(a) Planar Based (b) Bond-wire Based

Figure 1.12: 3D Models of Planar and Bond-wire Based Matching

3-D, and S-parameters are obtained. Then, an area with a length of 640 μm and width of 140 μm is allocated for compensation as shown in Figure 1.13. Afterward, this area is divided into equal-length parts, and these dimensions are optimized in 2-D simulation by minimizing the RL objective function. The wide-band RL and IL results are noteworthy with respect to the previously mentioned research. Despite that, this work uses 10 μm length matching sections and the same gap between signal and ground planes. The final model is not manufactured because PCB applications require at least three mils (76.2 μm) dimensions on all edges.

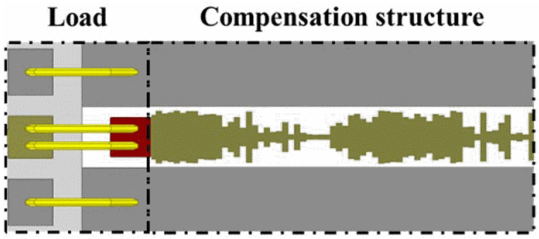


Figure 1.13: Compensation Model Dimension Optimization [22]

This thesis proposes a method that covers the PCB and interconnection process choices from the beginning to the end of the compensation network optimization. Minimum dimension limits from manufacturing capabilities and maximum dimension limits from multiple channel restrictions are obeyed to have a solid final design. The new compensation circuit provides convenience for size variations in the length and width directions. It reduces the simulation time significantly while keeping the result robust. Moreover, this matching design is scalable for different types of interconnections.

1.3 Contributions and Novelties

The contributions of this thesis are as follows:

- Usage of the proper substrate at E-band including optimum finishing type and via distribution
- Application of a die within (on top of) the PCB, especially at 77 GHz
- Utilization of compensation structures like grooving and ribbon followed by minimization of the distributed matching structure
- A hybrid circuit model that includes a W-element model of matching sections, asymmetric discontinuity models, and mutual capacitance
- Width and length optimization of distributed lines by using particle swarm optimization (PSO) in MATLAB

1.4 The Outline of the Thesis

This study involves three main topics: the theoretical background of low-noise amplifiers at E-band, design methodology, and optimizations.

Chapter 2 covers the understanding of LNA fundamentals, where operational and fractional BW are the origin points. Then, the noise sources and cascaded NF are described by using Friis transmission formula. Since the work is done in the E-band, where every detail tremendously affects the overall result, process challenges occur in both PCB and interconnection structures. Each aspect is elaborated to achieve a robust, reliable, and repeatable result.

Chapter 3 includes the primary design methodology behind the whole process. This is initiated by selecting and modeling the integrated circuit that is used with the PCB structure. It is pursued by EM simulations where excitation port definition alters the response of the building block. This port characterizes the boundary conditions that define how EM energy enters and exits the simulation domain. The very first step is finding the culminating RL and IL through TLs, as in every microwave application.

Afterward, the interconnection between the die and PCB is modeled that sidles with its compensation structures.

Chapter 4 describes how the previous steps are combined in an optimization manner. This is fed by through line, interconnection, and matching building blocks. Extracting the per unit length coefficients of each part can be analytically manipulated to achieve pairing between sections, including RLGC. This means that simulation time is decreased, and a more comprehensible recursion is established. After the successive implementation of modeling, it is continued with an optimization algorithm whose inputs are maximum space limitation and minimum manufacturing dimensions. The compensation network has been designed for varying width values of capacitive and inductive sections. The algorithm includes intermediate width values for these sections, which results in a more compact design thanks to on-target impedance transformations.

Chapter 5 concludes this thesis by reviewing and summarizing all aspects given in previous chapters. It also involves future work that would build on the knowledge gathered in this study.

CHAPTER 2

LOW NOISE AMPLIFIERS AT EXTREMELY HIGH FREQUENCY BAND

2.1 Low Noise Amplifier Essentials

As stated in the motivation section, the LNA is an inevitable part of radio RX architectures. A low noise and medium-high gain RF amplifier is required independent of the category, such as tuned radio frequency, direct conversion, or superheterodyne. Since the received signal levels are deficient ranging from -120 to -100 dBm and arduous to distinguish from the noise, the SNR should be kept under control [23]. The SNR expression is given by Equation (2.1).

$$(SNR)_{dB} = 10\log_{10}(\frac{P_{signal}}{P_{noise}}) \tag{2.1}$$

Although it is impossible to improve the SNR value after receiving, the LNA component degrades the SNR minimally.

2.1.1 Operating Frequency and Fractional BW

The operating frequency for LNA is chosen as 76-81 GHz due to the limitation of the transceiver, thus the nominal BW is the difference between start and stop frequencies which yields 5 GHz. Another vital measure, namely fractional BW, is determined by the ratio of the nominal BW and the geometric mean of the first and last frequencies [24]. In this case, BW is given by Equation (2.2).

$$BW_{frac} = \frac{|f_1 - f_2|}{\sqrt{(f_1 f_2)}} \tag{2.2}$$

When the 76-81 GHz values are inserted, the fractional BW is found to be 6.4 $\%$ approximately. In the lower frequency bands up to 10 GHz, this 6.4 percentage corresponds to a relatively narrow BW because the manufacturing range does not restrict the TL dimensions. By using the speed of light, the wavelength at the E-band is given by Equation (2.3).

$$\lambda_{unguided} = \frac{c}{\sqrt{f_1 f_2}} \tag{2.3}$$

When 76 and 81 GHz are applied in this equation, the unguided wavelength is found to be 3.8 mm. In subsection 2.2.1, the dielectric options are investigated in detail and a material with $\epsilon_r = 3.00$ is chosen. The square root of the value is inversely proportional to the wavelength, and the guided wavelength is updated to 2.2 mm. As stated in subsection 3.1.1, the chosen LNA has dimensions of 2.844 x 0.999 mm. Hence, the device itself is about one guided wavelength in the longitudinal direction. In the following sections, a distributed matching network is proposed, and one of the comparison parameters is the dimensions of the matching network with respect to wavelength [25]. A larger circuit not only increases the IL but also occupies more space, which is a drawback among other designs.

2.1.2 Noise Figure and Friis Formula

The NF can be defined as the degradation of the SNR between the input and output of any device as given in Equation (2.4). It is assumed by definition that the input noise power is the noise power produced by a matched resistor at T_0 = 290 K [26]. Once the noise is generated, it cannot be eliminated using other circuit components. If this NF is converted from dB to linear scale, it is called noise factor (F), as shown in Equation (2.5).

$$NF = \frac{S_i/N_i}{S_o/N_o} \geq 1 \tag{2.4}$$

$$NF_{dB} = 10\log_{10}(F) \tag{2.5}$$

Since the signal and noise are intermingled with each other, they are amplified and transferred together. Filter, power divider/combiner, attenuator, and phase shifter are passive components, and the noise level is directly equal to their losses. For active devices like amplifiers, oscillators, and mixers, the gain also affects the overall noise.

Hence, NF can be kept at a minimum by adjusting the quiescent bias point of active devices and external losses of passive devices. There are six primary noise sources in semiconductor devices, including thermal (Johnson), shot (Poisson), flicker (1/f), generation-recombination, burst (popcorn), and avalanche noises [4]. The thermal noise power depends on the temperature and BW as shown in Equation (2.6). When the temperature is 0 K, the random movement of electrons is stopped, and thermal noise is eliminated. Above the absolute zero, this noise type is directly proportional to the temperature. The same effect is seen for the BW case due to the gathering of more noise in the frequency range.

$$P_{thermal} = kTB \tag{2.6}$$

The flicker noise is a dominant one in the lower band and rapidly degrades with a frequency whose spectral density is given by Equation (2.7). This originates from surface traps and defects that temporarily capture and release free carriers (electrons and holes) in the material.

$$S(f) \propto \frac{1}{f^k} \quad , 0.8 \leq k \leq 1.2 \tag{2.7}$$

Shot noise arises because electric current consists of discrete charges (electrons) moving randomly. This randomness causes fluctuations in the current even when it is steady on average. This noise type follows a Poisson distribution given in Equation (2.8). In this formula, λ is the average rate of arrivals like photons per second or electrons per second, where n is the number of arrivals during a fixed time interval [27].

$$P(n) = \frac{\lambda^n e^{-\lambda}}{n!} \tag{2.8}$$

After defining the concept and types of noise, separate noise sources can be combined using the Friis formula. Friis noise formula states that the overall F of a cascaded system given in Figure 2.1 can be characterized by using individual F and gain/loss of each sub-system [4]. The F of the first stage is directly added, and F of all other stages are rationed by the linear gain multiplication of all the pre-stages as in Equation (2.9).

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... + \frac{F_n - 1}{G_1 G_2 ... G_{(n-1)} G_n} \tag{2.9}$$

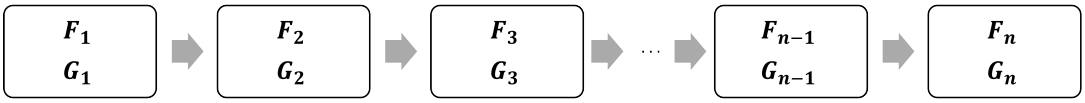


Figure 2.1: The Cascaded System Given By F and G Values

It is the analytical reason why every RX system requires an LNA as the first stage. When the initial component has a F_1, then the overall noise cannot be less than or equal to this value. This noise domination creates a solid basis for the primary motivation of this thesis. To be specific, the chosen transceiver IC component in this study has built-in mixers and intermediate frequency amplifiers. Its NF value is 13 dB, and a pre-stage LNA with a 3.6 dB NF is proposed to minimize the noise in the overall system. However, there are RF bonding connections and distributed matching networks, and the NF value deteriorates. According to the previous studies of Sumitomo Electric, the negative effect of the interconnection on the NF varies with the bond length [28]. For L = 0 μm (on chip), the NF changes between 3.5-4 dB in the 76-81 GHz band. For L = 300 μm, this value climbs up to 5.5-6 dB. If this NF = 6 dB of the worst (longest bond) case is applied to the aim of this thesis, the overall NF is still far better than the only transceiver IC scenario. While designing the interconnection and compensation, the 6 dB NF value is targeted for comparison.

2.2 E-BAND PROCESS CHALLENGES

As mentioned in the first chapter, there is still a lack of packaged transistors in the EHF band because of the die, printed circuit board (PCB), and interconnection limits. PCB limitations can be seen under different categories, starting from properly chosen permittivity, loss tangent, height, etc. Then, the finishing type directly affects the IL. Also, opening an optimum cavity within the first layers of PCB and proper placement of the die is another crucial point. In addition to PCB manufacturing, the interconnection between the die and PCB is also challenging. Wire-bond and ribbon-type transitions are available in different sizes and applications. The number of bonds, width, length, height, and inflection profile mainly characterize these connections. Also, it is required to ensure that these bonds can handle vibration, shock, drop, and pull tests because of their usage in moving vehicles.

2.2.1 PCB Substrate, Finishing, and Manufacturing Limits

In the lower frequency bands up to MHz range, the dielectric substrate is usually chosen as Fiberglass Reinforced 4, and the conductive finishing is generally preferred as ENEPIG. These serve well for high-power and easier soldering and re-work applications [29]. When the thermal load becomes too high to be dissipated by PCB surface and air convection, cavities are opened in PCB through all layers, and flanged transistors are screwed to a more extensive mechanical body as shown in Figure 2.2.

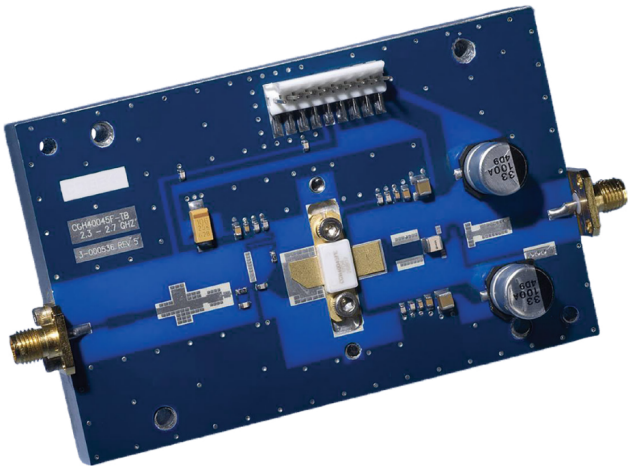


Figure 2.2: Flanged Transistor in All-Through Cavity on PCB [29]

However, in the EHF band, the IL value significantly increases with increasing frequency, as shown in Figure 2.3. Also, the permittivity and loss tangent values are given in commercial datasheets for a specific region, generally up to SHF [30]. More investigation is required to get these values from the substrate manufacturer, but the manufacturer could not even provide test values in some cases. In this case, an extrapolation method, namely the Djordjevic-Sarkar Method, can be used [31].

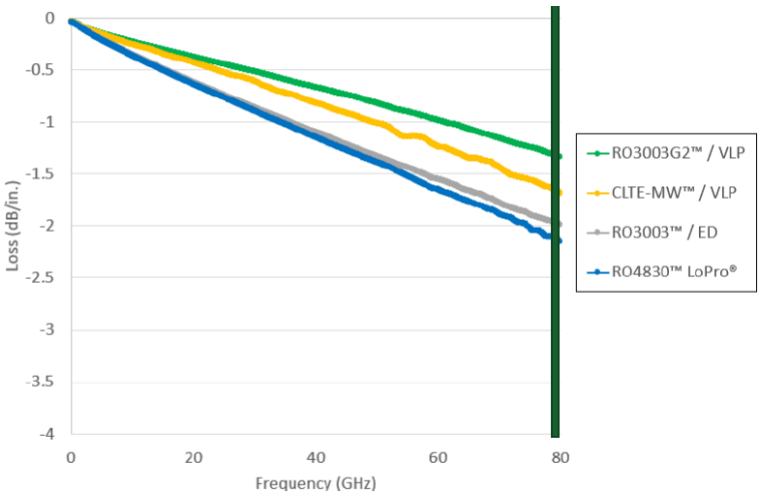


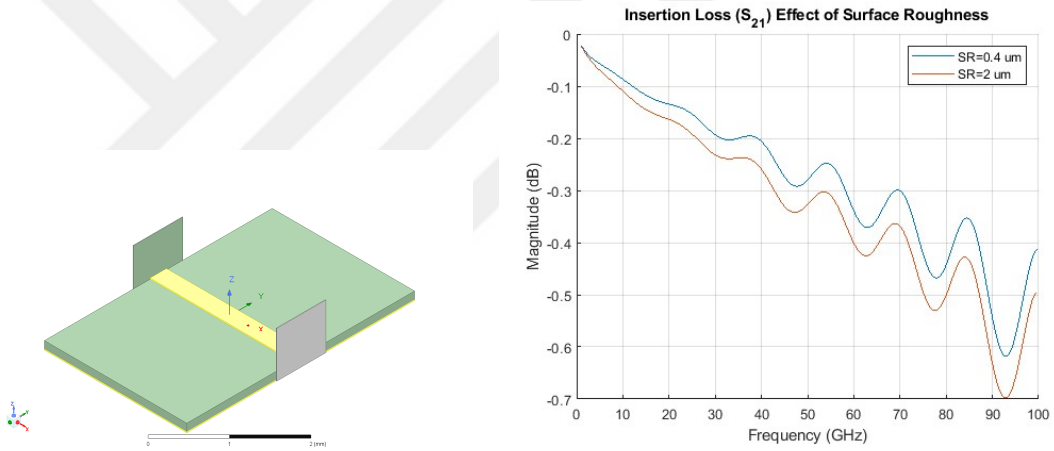
Figure 2.3: IL at 77 GHz [30]

The choice of substrate that carries the TLs is a critical design parameter from both RF and direct current (DC) perspectives. This preference determines the maximum thermal load capability in the first place. According to thermal load specification, the substrate should be chosen so that it is not flammable under these conditions. After the choice of dielectric material considering thermal management, the next step is determining the height of the substrate, which constrains both the mechanical endurance and TL dimensions along with the impedance and propagation delay. Based on the requirements of low height, low tangent loss, and invariant permittivity, there are mainly three different options. These are liquid crystal polymer of Micro System Technologies, RO3003 of Rogers Corporation [32], and Astra MT77 of Isola Group [33]. Considering the loss tangent comparison given in Table 2.1 and LNA die height of 50 μm with an additional 25 μm height of epoxy, the proper substrate is chosen as RO3003.

Table 2.1: Comparison of Dielectric Substrates

Properties	MST LCP	RO3003	Isola Astra MT77
Relative Permittivity (ϵ_r)	2.9	3.00 @ 40 GHz	3.00 @ 10 GHz
Loss Tangent (tan δ)	0.0025	0.0010	0.0017
Minimum Thickness	25 μm	127 μm	63 μm

There are standard cladding options for RO3003 material, namely electro-deposited and rolled copper foil. The electro-deposited one is easier to manufacture and has a lower cost, which makes it a good candidate for moderate applications. However, surface roughness (SR) is also essential at 77 GHz application, and rolled copper foil should be used [34]. This effect is also embedded on top of the thorough TL modeling. In this scenario, the substrate material is chosen as RO3003 with 127 μm height with previously given RF characteristics. A 287 μm width and 2.5 mm length microstrip line with extended wave ports. The SR values of rolled copper (0.4 μm) and electro-deposited (2 μm) are taken from Rogers metal cladding document [35]. A simulation with a solution frequency of 100 GHz is swept between 0-100 GHz range. The SR values are realized by assigning advanced finite conductivity boundary in HFSS, and the results are given in Figure 2.4. There is a 0.1 dB change in RL at the EHF band for these two different SR values.



(a) 3D Model

(b) IL Effect

Figure 2.4: SR Analysis

Another essential property of a PCB design is the finishing type. The manufacturer provides a panel or sheet of substrate with copper coverings on both sides of the dielectric. Although copper has a high electrical conductivity of $5.8{\cdot}10^7$ S/m with respect to gold ($4.5{\cdot}10^7$ S/m), it is not preferred for direct use. Because gold is soft and pliable, it may be used to create flawless contact surfaces that are perfect for soldering and mechanical connections. Also, gold exhibits exceptional wear resistance

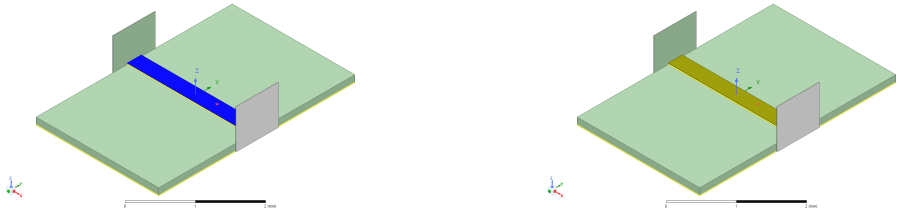
when alloyed with trace amounts of other materials (such as nickel), which makes it appropriate for contact pads and connections that are subjected to frequent mechanical stress [36]. There is also a silver finishing option on top of the copper, but silver has a tarnishing problem. The manufactured PCB should be kept under vacuum sealing and low moisture conditions until the soldering process is started. The low-frequency PCBs are generally finished with ENEPIG to ease the soldering re-work process of surface mount devices. The Ni and Pd elements are used in the standard manufacturing process to increase durability and allow lead-free implementations.

After the examination of the literature and realization of EM simulations, it is seen that both Pd and Ni of ENEPIG finishing negatively affect the IL of the TLs as shown in Table 2.2 [37]. This loss is sourced from the resistive conduction and should be worked separately from the dielectric losses of the substrate. Since the loss value is vital in the EHF band, it has been decided to continue with either plain gold or silver finishing, depending on the other parameters.

Table 2.2: Comparison of the IL of Surface Finishes

	IL (dB)			
Frequency (GHz)	ENEPIG	ENIG	EPIG	IGEPIG
10 GHz	-5.1	-5.1	-3.4	-3.5
20 GHz	-8.6	-9.1	-6.5	-6.6
30 GHz	-12.5	-13.3	-10.3	-10.4

While Table 2.2 shows research in the literature, a 3D HFSS modeling is studied to see the effect of additional finishing elements. The through TL model is covered with Ni and Pd as seen in Figure 2.5. Similar to the SR case, the solution frequency is 100 GHz, and the frequency sweep is from 0 to 100 GHz. The line width is 287 μm with extended wave ports, and the line length is 2.5 mm. Comparative results are given in Figure 2.6. It is seen that the IL gets worse by 0.3 dB at 80 GHz for a 2.5 mm through line.



(a) Nickel Plating on Top of Gold (b) Palladium Plating on Top of Gold

Figure 2.5: Nickel and Palladium Plating Models

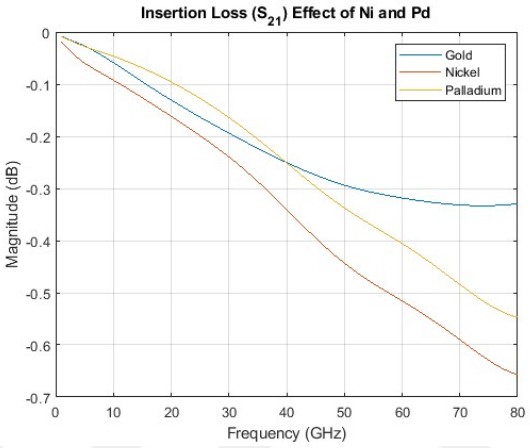


Figure 2.6: IL ($|S_{21}|$) Effect of Ni and Pd

In addition to the literature search and simulation, the effect of PCB finishing is investigated by measuring the S-parameters of the throughline PCB design. The millimeter-wave network analyzer system of Keysight is used in the measurement setup of the through lines. It consists of N5261A and N5251-90001. It works from 10 MHz to 110 GHz with extensions up to 1.1 THz. Since this network analyzer works at E-band frequency, calibration and verification are required. A 1 mm calibration and verification kit of 85059A is used to meet the specifications. The very first manufactured PCB has two different lengths through the TL. It relies on the suggested coplanar waveguide (CPWG) structure with 213 μm signal width and 102 μm ground gap. The shorter one has a length of 11.65 mm, while the longer one has 16.65 mm. The dielectric has standard electro-deposited copper and has worse SR compared to rolled copper. The finishing op top the PCB is standard ENEPIG as shown in Figure 2.7.

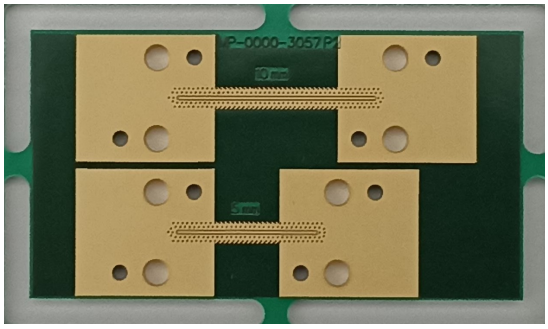
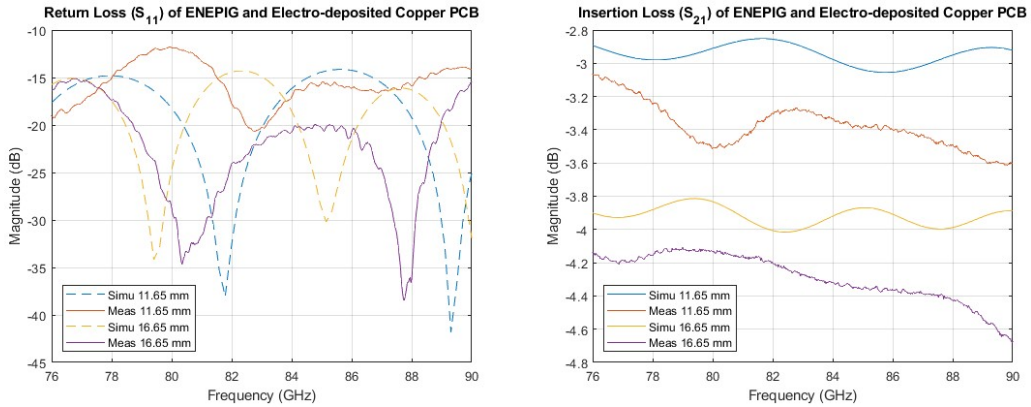


Figure 2.7: ENEPIG and Electro-deposited Copper PCB

The resultant RL values are compared with respect to the line length. It can be seen that the $|S_{11}|$ value is better in most of the frequency bands. However, it can be misleading because of the non-reflected lost signal power. Hence, IL values are compared as in Figure 2.8 after connector losses are de-embedded by the differential length method. From these results, it is concluded that ENEPIG and electro-deposited copper PCB have IL per unit length of 0.205 dB/mm.



(a) RL ($|S_{11}|$)

(b) IL ($|S_{21}|$)

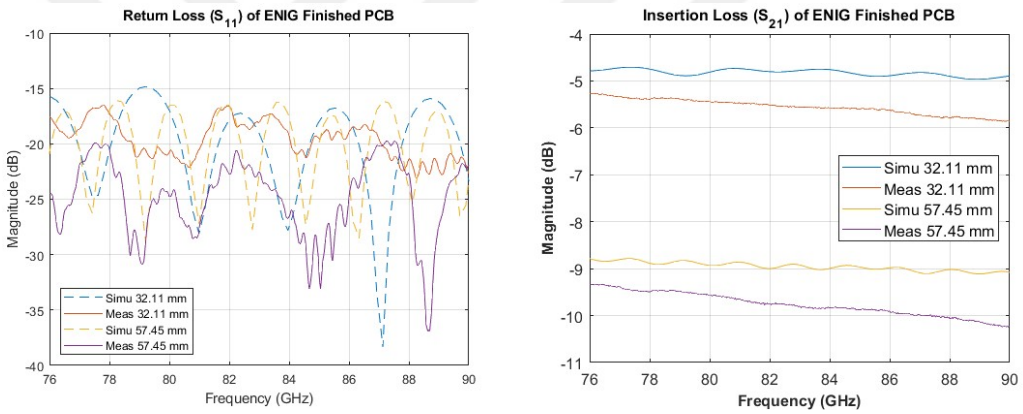
Figure 2.8: S-Parameters of ENEPIG and Electro-deposited Copper PCB

The second manufactured PCB has the same signal width and gap. In this case, the shorter line has a length of 32.11 mm while the longer one has 57.45 mm, as shown in Figure 2.9. The finishing op top of the PCB is changed to EPIG by eliminating the nickel plating process.



Figure 2.9: ENIG Finished PCB

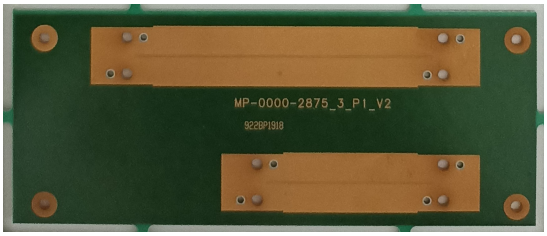
Then, resultant RL and IL values are compared as in Figure 2.10 after connector losses are de-embedded by the differential length method. From these results, it is concluded that ENIG finished PCB has IL per unit length of 0.148 dB/mm.



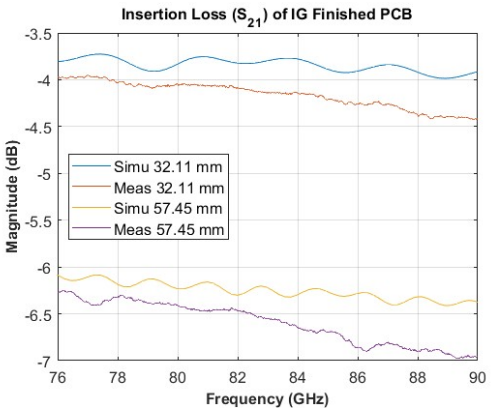
(a) RL ($|S_{11}|$) (b) IL ($|S_{21}|$)

Figure 2.10: S-Parameters of ENIG Finished PCB

The third manufactured PCB also has the same signal width and gap. Line lengths are 32.11 and 57.45 mm, as shown in Figure 2.11. The finishing op top of the PCB is changed to IG by eliminating both the nickel and palladium plating process. Then, the IL values are compared after connector losses are de-embedded by the differential length method. From these results, it is concluded that IG-finished PCB has IL per unit length of 0.094 dB/mm.



(a) Manufactured PCB



(b) IL ($|S_{21}|$)

Figure 2.11: IG Finished PCB and Results

Besides the substrate selection and finishing types, minimum limits also arise from manufacturing limitations. As a CPWG structure example, the minimum width and spacing values for the conductive plane shown in Figure 2.12 are limited by 76 μm (3 mils). On the left, there is a 50 Ω line with intermediate width w_1. There are narrow inductive w_2 and wide capacitive w_3 sections and ground plane gaps of g. This restricts the maximum inductance value of the narrow section by limiting the w_2 dimension in the figure. Also, this limit determines the minimum length of each inductive section in the multistage compensation because there should be at least $g + g + g = 229$ μm length of inductive section caused by signal and ground plane proximity from capacitive sections on the right and left-hand sides.

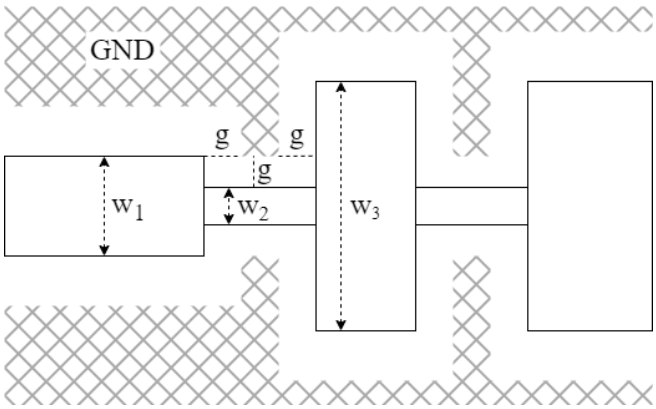


Figure 2.12: CPWG Distributed Matching Limitations

2.2.2 Interconnection Types, Effects, and Parameters

The die components have conducting signals and ground pads on top of them. The fundamental interconnection between the die and PCB is wire-bond and ribbon for the time being [38]. Wire-bonding is the method of connecting gold wire to two points in a structure to create a connection or a pathway for electricity. Figure 2.13 shows the fundamental parameters for the general case of bonding [21]. There is a substrate material of PCB with ϵ_1 permittivity and h_1 height, whereas the die component has ϵ_2 and h_2. Both of the bottom ground planes of the die and PCB are connected with vias. The die has a signal pad on the top with a surface area of A, which restricts the maximum width (diameter) of the bonds. Also, there is a TL end on the PCB that is wider than the die because of the lower permittivity with respect to the die. These two points are interconnected by a gold bonding whose main design parameters are its height h_{wb} and length L_{wb}. In the literature, there are studies that conduct the parametrization of interconnection dimensions. One of them shows that the signal trace width for the 50 Ω, the gap between the chip and PCB edge, chip-PCB level difference, wire-bonding height, and length are highly effective in terms of S-parameters, especially in EHF band [39]. Besides the wire bond, the other type of interconnection is called ribbon, which indicates a combination of thinner structures into a wider material. Ribbon wedge bonding can transmit higher currents and is more sensitive to delicate GaAs bonding pads.

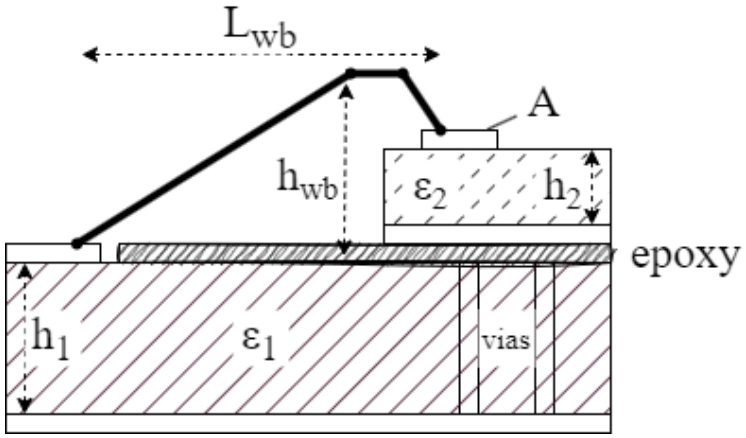
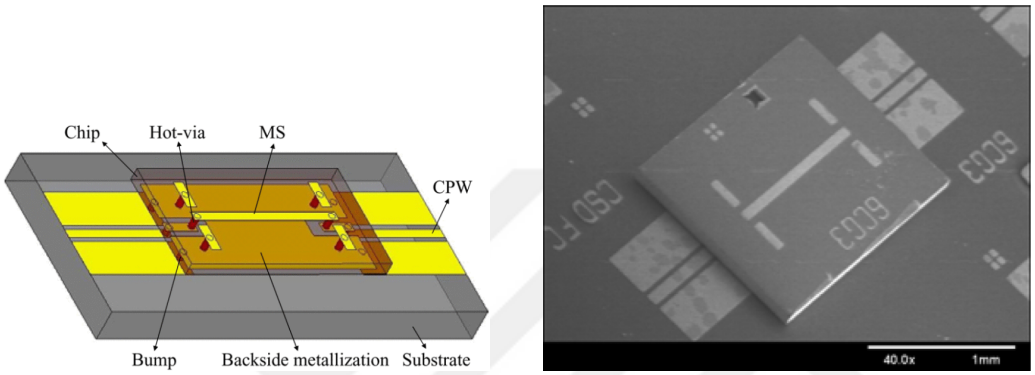


Figure 2.13: Wire-Bond Model Side View

This area is evolving to find better solutions like hot via, which is a concept of drilling and plating from top layer pads to the bottom layer of the die as depicted in Figure 2.14. The hot via is an alternative process for wire-bond and ribbon to decrease interconnection losses and is used in the literature. In a 60 GHz design, the PCB substrate is chosen as 254 μm Al_2O_3, and the chip is designed over 100 μm GaAs with a 3 mm length microstrip line. After manufacturing and measurement, the IL of the interconnection structure is given as 0.22, 0.32, and 0.49 dB for 20, 40, and 60 GHz, respectively [40].

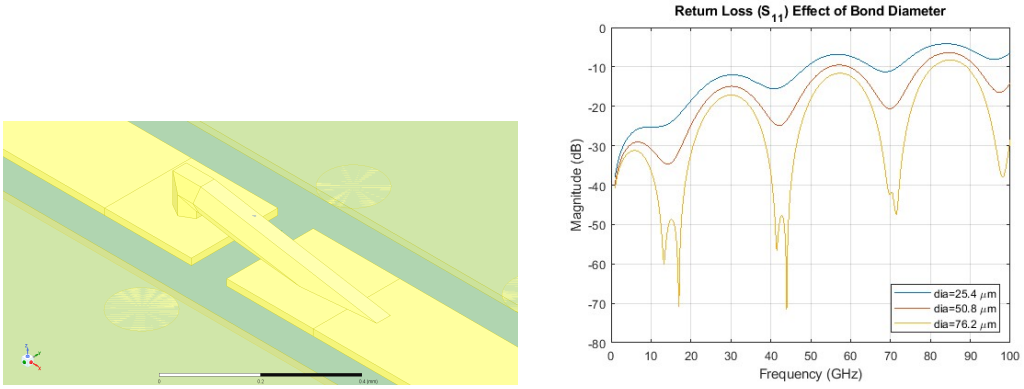


(a) 3D Model

(b) Manufactured PCB and Die

Figure 2.14: Hot Via Implementation [40]

This hot via application is available when the internal structure of the MMIC can be designed. In this thesis, only the wire-bond and ribbon solutions are modeled and compared because the die component is taken from ready-to-use options. Since the chosen die has conductive routing in interlayers, the hot via technique is not compatible. As stated in the proposed method section, the ribbon bonding improves both RL and IL performances. A ribbon can be intuited as a thicker version of the bond, as shown in Figure 2.15 to see the effect of changing the bonding types. The diameter of the bond is initiated from 25.4 μm, which corresponds to a standard one mil wire bond. Then, the diameter is linearly increased by factors of 2 and 3 since the standard ribbon bond is three mils in diameter. All results are compared and it is seen that both the maximum and minimum points in the RL are improved with increasing diameter. This RL improvement occurred owing to both the increment in the signal flow path width and the decrement in the total parasitic inductance by paralleling.

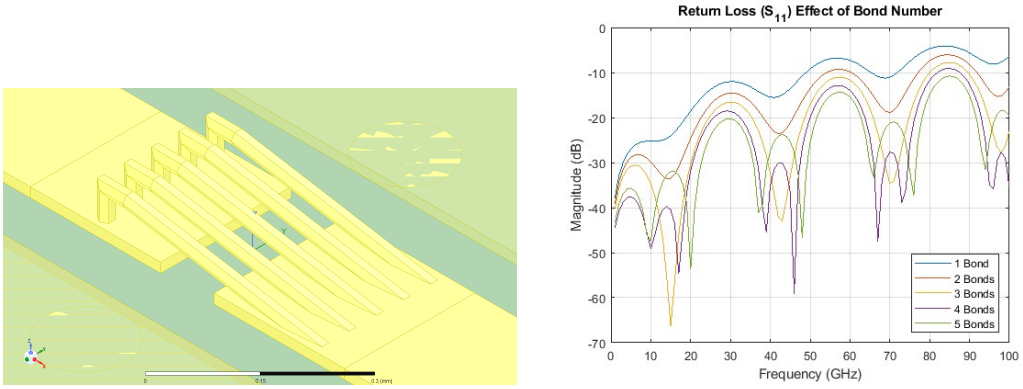


(a) 3D Model

(b) (S_{11}) Effect

Figure 2.15: 3D Model and Results of Bond Diameter

There are four main parameters that characterize the interconnect: the number of bonds, length, height, and inflection profile. According to the literature research given in the proposed method section, the shorter, shallower, and maximum number of bonding minimizes the negative effect of the interconnect [13]. The chosen die has 72 μm width and 76 μm length, and these dimensions determine the scope of the bond manufacturing process. This forces the user to use either, at most, two wire bonds with one mil diameter or one ribbon with three mil diameter. The length, height, and inflection profile topics are covered in the following chapter, specifically for the die properties. Still, the effect of several bonds can be generally studied for this part. In Figure 2.16 the number of bonds is increased to five, and the change of RL value is shown for bond numbers from 1 to 5 gradually. Similar to the bond diameter comparison case, the RL values are improved with increasing bond number. The RL improvement is caused by a similar reason where the input signal can be transmitted by multiple bond cross-sections, and the inductive parasitic effects are decreased by paralleling.



(a) 3D Model

(b) (S_{11}) Effect

Figure 2.16: 3D Model and Results of Number of Bonds

2.2.3 PCB Cavity Limitations

As stated in the introduction, a bare die component lacks packaging and molding, and it should be directly bonded to the PCB. The main aim of the interconnection process is to minimize the bonding dimensions. A cavity is required to compensate for the height difference between the substrate and the die surfaces. If the die were directly attached to the surface, this difference would increase, and the wire-bond length also increase, resulting in more reflections. If the substrate to be etched has thicker layers compared to the die height, then the interconnection dimensions increase. A similar problem happens if the die is placed on the lowest ground level in a multi-layer PCB. These two extremum points identify why a cavity with a proper height is required. In this study, the chosen die has 50 μm, and the substrate has 127 μm heights, while the binder between them helps balance these values.

In addition to the height effect, there are also width and length constraints from the manufacturing. There is a proximity limit between the edges of the die and edge plating walls inside the cavity. The die should be closer to the PCB edge without short-circuiting components to achieve smaller interconnections with better RF performance. This proximity minimum varies from 51 μm to 127 μm (2 to 5 mils) depending on the capabilities and the manufacturing cost. A shift parameter is defined for a nominal cavity model as seen in Figure 2.17 to see the effect of the placement of die in the cavity. In this figure, a thin blue box represents the die and is placed

at a distance from the opened cavity within the gold-finished PCB. There are 50 Ω through lines on top of both RO3003-based PCB and GaAs-based die. Also, there are signal and ground bonds with three mil thickness.

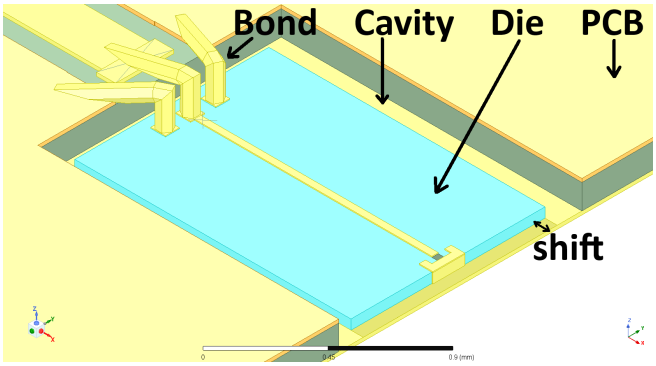


Figure 2.17: 3D Model of Shifting the Die within the Cavity

When the shift of the die within the cavity parameter is swept, its RL effect is observed as in Figure 2.18. It is seen that the RL can be affected by up to 3 dB in the EHF band by changing the position of the die in the x-y plane. In some cases where the die x-y dimensions are relatively larger, and junction temperature is problematic, the cavity is opened all through the PCB like in the screwed flange. Then, a sensitively manufactured copper or gold coin is inserted below the die for the solution of both height difference and heat dissipation.

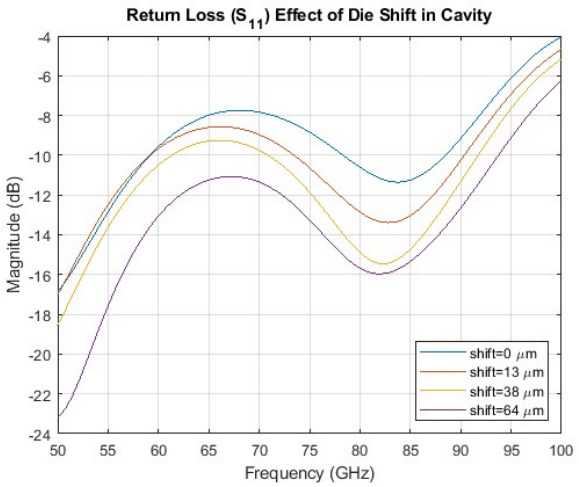


Figure 2.18: Return Loss (S_{11}) Effect of Die Shift in Cavity

CHAPTER 3

DESIGN METHODOLOGY

The model parameters in the higher frequency bands should be determined carefully because they significantly affect the overall result with respect to the lower band. The choice of die component is crucial in terms of electrical properties and mechanical implementation. Also, the modeling of the 3D EM structures requires proper port definition and placement of vias. Especially in the die-on PCB design, the wire-bond or ribbon models should be similar to the actual implementation to have consistent results.

3.1 Building Blocks: IC and PCB

Two main constituents construct the design. One of them is the bare die, and the other is the PCB. Both of them are modeled in the Ansys HFSS program [7]. Their stand-alone characteristics and interactions are studied in detail.

There are a few E-band LNA products currently available in the marketplace. After investigation, SMM5727XZ of Sumitomo Electric, which is a five-stage GaAs MMIC that operates between 71 and 86 GHz, is found. This product uses wafer level chip size packaging (WLCSP) technology with solder balls as shown in Figure 3.1. It has typical features of 20 dB G, 5 dB NF, and an output power of 11 dBm at 1 dB gain compression [41]. This flip chip die can be used in the solder reflow process, but the product is not on sale.

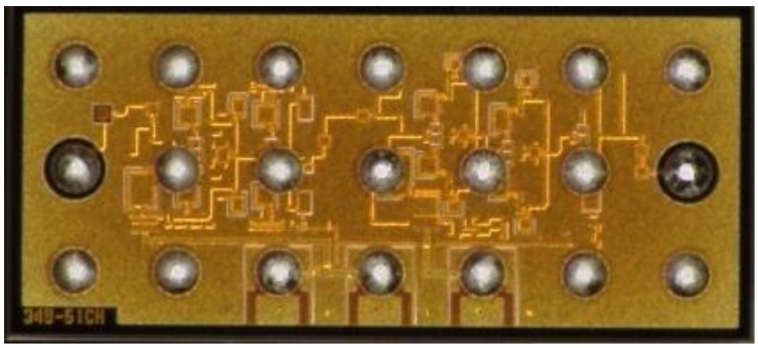


Figure 3.1: SMM5727XZ Product with WLCSP Technology [41]

Other candidates come from MKR-Technologies TeraHertz chip list. There are MKR-60LNA, MKR-65LNA, MKR-70LNA, and MKR-75LNA. MKR-60LNA and MKR-70LNA are relatively narrow-band, while MKR-65LNA and MKR-75LNA are broad-band devices. MKR-60LNA and MKR-70LNA provide better G and NF but worse BW and compression. Since MKR-65LNA and MKR-75LNA products are broad-band, they cannot contribute to a high output saturation power [42]. All details are given in Table 3.1.

Table 3.1: Comparison of MKR-Tech TeraHertz Chip List

Properties	MKR-60LNA	MKR-65LNA	MKR-70LNA	MKR-75LNA
Freq (GHz)	60-90	65-110	70-90	75-110
Gain (dB)	21	20	25	22
NF (dB)	3.2	2.3	2.9	3.6
OP_{1dB} (dBm)	10	0	9	0

The HMC8325 is an E-band GaAs MMIC LNA chip that operates from 71 GHz to 86 GHz. Detailed RF properties of the die are given in the datasheet. Fundamental properties are G = 21 dB, NF = 3.6 dB, and size of die size: 2.844 mm × 0.999 mm × 0.05 mm. However, routing and 3D models are not available. Routing is investigated under the microscope after the purchasing process, as shown in Figure 3.2. The inner layer structures will be examined to see if the sectionalization can be realized successfully. The 3D model is constructed by width, length, height, and

pad dimensions where upper and lower conductive surfaces are created as 5 μm gold plating. There are two RF signals and four ground (GND) pads on top of the die. There are 16 distinct DC pads, half of which are internally grounded. The die uses four cascaded stages corresponding to four gates and four drain pins, while the first two and last two stages are connected internally.

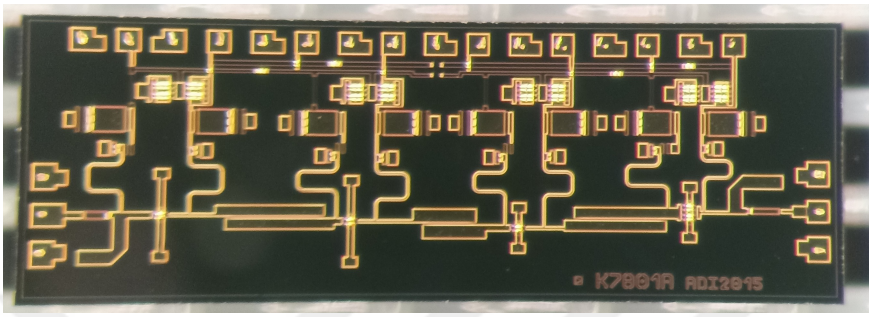


Figure 3.2: HMC8325 Product Under Microscope

Another design choice is PCB selection. RO3003 high-frequency circuit materials are ceramic-filled poly-tetra-fluoro-ethylene composites designed for commercial microwave and RF applications. This product line was created to provide outstanding electrical and mechanical stability while remaining cost-effective. The dielectric constant of this substrate is given between 3.12 and 2.97 for the 8-40 GHz frequency band. Additionally, the dissipation factor is given as 0.0010 for only 10 GHz. For the intersection of these two values at 10 GHz, an extrapolation is used, relying on the Djordjevic-Sarkar Model. The substrate has a height of 5 mil (127 μm) +/- 0.5 mil tolerance and is covered by 18 um gold on both sides.

3.2 Numerical Modeling

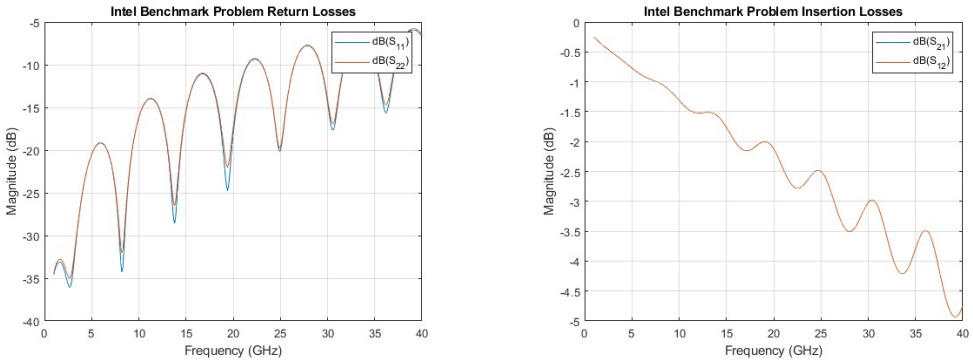
In the EM simulation environment, Ansys HFSS and CST Studio Suite are two dominating programs where that have different interfaces but similar solution algorithms [43]. In the following subsections, HFSS is used for numerical modeling.

3.2.1 Port and Transmission Line Definitions

There are seven types of excitation in HFSS, and wave and lumped ports are actively used in this study. All excitation types generate field information, but only wave ports, lumped ports, and Floquet ports provide S parameters. Wave port is a frequently used excitation type in HFSS. They are ideal for exciting microstrip, stripline, coaxial, or waveguide TLs. Wave ports should only be applied to the outer face of the solution space. The lumped port functions similarly to a current sheet source and can be used to excite standard TLs. It has the advantage of de-embedding the parasitic created around the input and output points. Despite that, the wave port is proper when auxiliary line extensions are required. In this way, the user can create longer through lines at the beginning and end of the framework to subtract the effect later. This is necessary to ensure that evanescent and unwanted EM modes are already diminished when the signal reaches ports.

This study started by using the lumped port approach in the through TL and wire bond compensation structures. Later on, the wave port became necessary for an implementation to get reliable results in the cascading blocks method.

The very first step to RF numerical modeling is determining the type of TL, continuing with the characteristic impedance Z_0. The die architecture does not allow either coaxial, twin-axial, or tri-axial cable waveguide or stripline TLs. Hence, the line design is based upon two other types: micro-strip line and coplanar waveguide with ground (CPWG). At this point, there should be a reference point to check whether the through TL modeling is correct or not. Intel Benchmark Problem gives a solid idea about which type of response is expected when the setup is appropriate [44]. In this work, the relative permittivity (@ 5 GHz) of the dielectric is 3.4, the loss tangent of the dielectric is 0.018, conductivity is 4.5 $\times 10^7$ S/m, SR is 0.3 μm, and ϵ_r and tanδ of the solder resist are 3.4 and 0.027 respectively. The dielectric thickness is 20.72 μm whereas ground copper thickness is 17.5 μm and TL thickness is 15.63 μm. The TL width is 29.62 μm and has a length of 14.85 mm. The last parameter of solder resist thickness is 33.55 μm. This model results in repetitive and decaying RL and IL between 1 - 40 GHz, as shown in Figure 3.3.



(a) RL of Benchmark

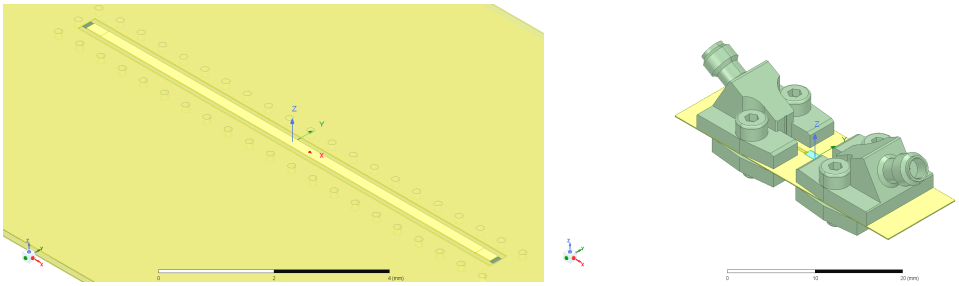
(b) IL of Benchmark

Figure 3.3: Intel Benchmark Problem RL and IL

Initially, the bottom ground plane, substrate, and upper signal plane are modeled in the analysis. Since the conductor and dielectric heights are already defined, the remainder of the design parameters are signal line width and upper ground plane distance. The first attempt is based upon two recommendations from transceiver IC and RF connector application notes. mmWave Radar Sensor RF PCB Design, Manufacturing, and Validation Guide of TI state optimum ball grid array to PCB transition and CPWG dimensions given in the application note [45]. This proposes a signal line width of 213 μm, signal to ground gap of 102 μm, and via pitch of 717 μm along the two sides of the signal pad when RO3003 material is used. Via drill-pad diameters, horizontal via distance, and stagger in the second row are given for the general case.

Another suggestion arises from 01K80A-40ML5 of Rosenberger right angle jack PCB launcher product [46]. The contact area of the pin is recommended to be a rectangle of 0.2 mm width and 0.35 mm length. The plated through holes with 0.2 mm diameter and 0.4 mm pitch are advised, and proper mounting should be done by adjusting the connector pin to the middle of the PCB line.

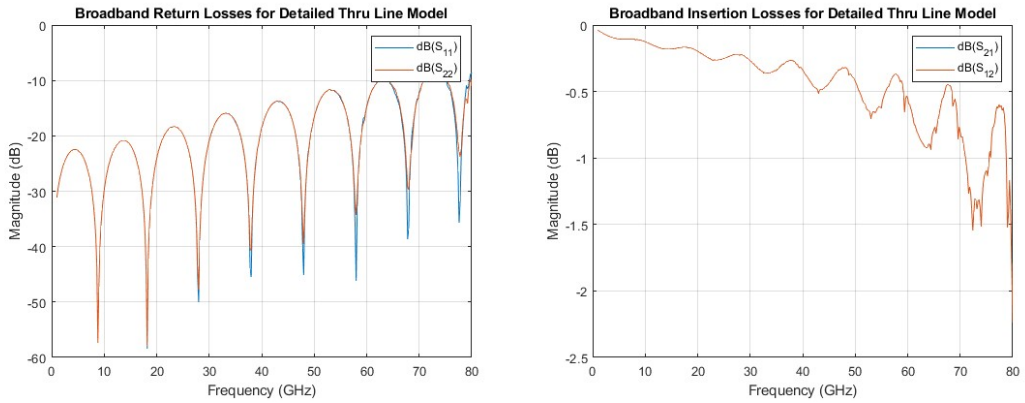
Combining these two pieces of information, an HFSS model is created where the via diameter is 150 μm, and the center pitch is 525 μm. This model uses the standard and constant substrate parameter definitions like ϵ_r = 3.00 and tan δ = 0.0010. To reduce the simulation time, empty spaces reserved for the connector shown in Figure 3.4 are deleted.



(a) 3D Model Based On Datasheets (b) Connector Placement on PCB

Figure 3.4: PCB and Connector Dimension Comparison

The driven solution setup is changed so that the adaptive solutions (meshes) are generated according to the 100 GHz frequency in order to create a necessarily sensitive meshing distribution. Once the procedure is completed, a simulation in narrower band (74-80 GHz) is run. It shows an undisturbed waveform starting and ending with a -10 dB RL while having a -39 dB resonance at 77.65 GHz. After examining this anticipation, the same model is simulated in the wide-band (1-80 GHz). With eight distinct resonances as depicted in Figure 3.5, the outcome matches with the reference point. Correspondingly, the IL value starts from almost 0 dB and drops down to -2.5 dB at the end of the band. Since the structure is passive and physically symmetrical, $S_{11} = S_{22}$ and $S_{21} = S_{12}$ hold.



(a) RL of HFSS Model (b) IL of HFSS Model

Figure 3.5: Broadband S-Parameters for Detailed Thru Line Model

Another helpful tool is Q2D. In this type, the user only defines the cross-sectional view of the desired PCB. The length of the TL is out of concern, and only thickness and width are required for the characterized materials. To double-check the dimensions, a two dimensional (2D) model is constructed where the bottom ground plane width is equal to the connector and the PCB width is 10.9 mm. There is a complete RO3003 model with five mils (127 μm) height, which carries one signal line of width 213 μm and two broad coplanar ground planes at a distance of 102 μm. Since the via has a cylindrical form in 3D, its projection into the 2D model is a rectangle whose width is via diameter as demonstrated in Figure 3.6.

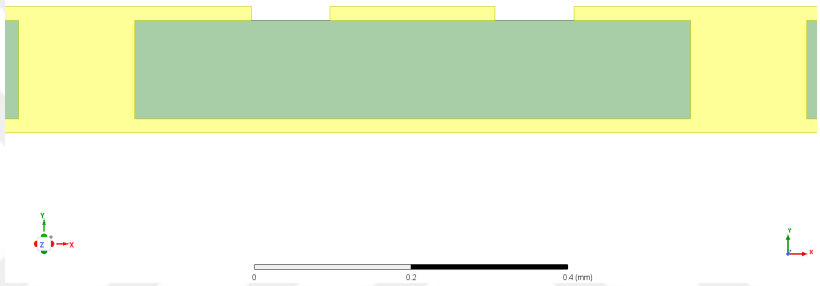
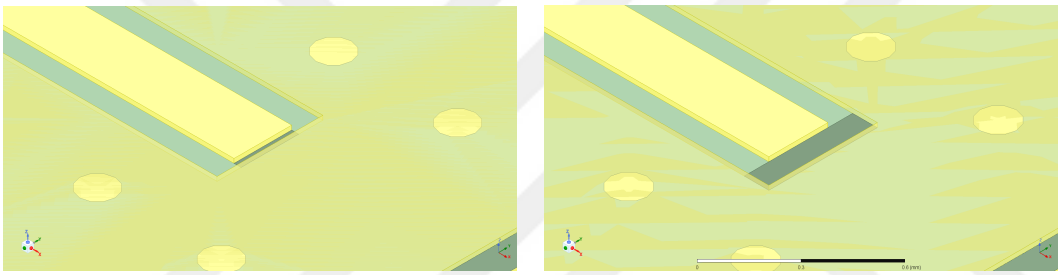


Figure 3.6: Complete Q2D CPWG Structure

The excitation mechanism is a bit different in this case. There are no lumped or wave port options, but it directly assigns conductors to signal, reference ground, and floating ground. Since the upper and lower ground planes are connected, they are combined into a comprehensive one. The optimum Z_0 = 50 Ω impedance in Q2D is achieved with 287 μm width in micro-strip and 244 μm width - 102 μm gap in CPWG. The grounding effect for three more different cases is inspected in Q2D. The first one is moving the via cross-sections to each end of the model. Another one is discarding the via but defining floating grounds on the upper coplanar areas. The last one is eliminating both the via and the coplanar floating grounds. In each case, including the nominal one, the characteristic impedance varies for different frequencies. Even if the vias are in the furthest position, the coplanar grounding still works, and these two results are similar. On the other hand, defining floating grounds changes the impedance, as in the case of only bottom grounding.

After finding the necessary line width values in the Q2D, these lines are modeled in a 3D workspace, and proper environmental conditions, including port definitions and via distribution, are applied. From the port definition perspective, the length of the port is defined by the user. The first thing that springs to mind is equating it to the width. However, since there is a constrained gap between signal and ground in the CPWG structure, it might create a problem since this gap is not equal to the width. Then, the second alternative for port distance emerges as equating it to the signal-ground gap. This dimension is parameterized, and its effect is observed in the simulation results.

The length of the port is parameterized and decreased to a smaller one. The width of the lumped port might be directly subjected to the TL width restriction, but it is also tried to widen the port until it touches the side ground planes as in Figure 3.7.



(a) Decreasing Port Length

(b) Increasing Port Width

Figure 3.7: Effect of Port Dimensions

When the results given in Figure 3.8 are investigated, it is seen that neither decreasing the port length nor increasing the port width improves the RL when compared to the nominal case where port length is equal to signal gap and port width is equal to signal width.

The minimum via diameter is found as 150 μm from different manufacturer sources. The via distribution distance is started from the rule of thumb $\lambda/10$ distance, and this pitch distance is decreased gradually until the minimum manufacturing limits. For example, the via just behind the ports is crucial to ensure that the field is distributed correctly. The second row of vias and more rows than two are also simulated. However, the first and second ones seen in Figure 3.9 are found to be necessary and suf-

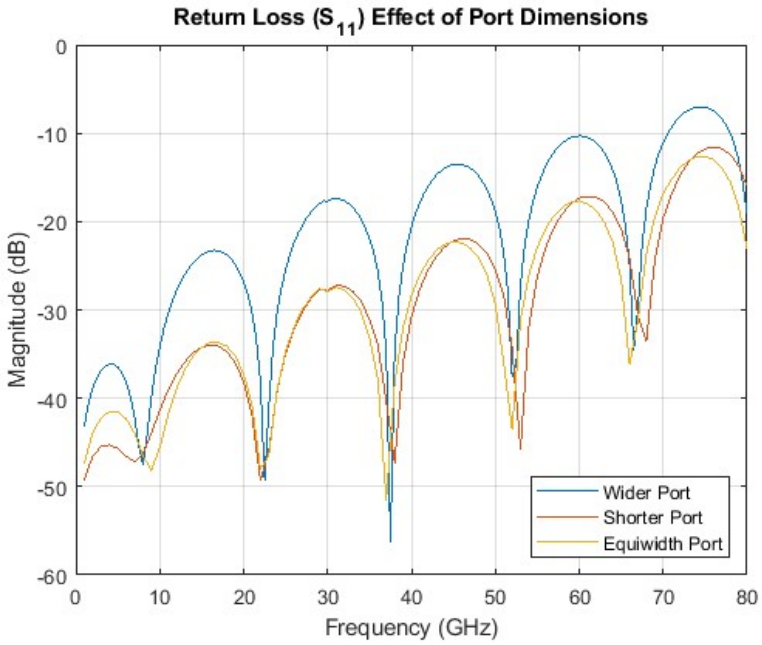
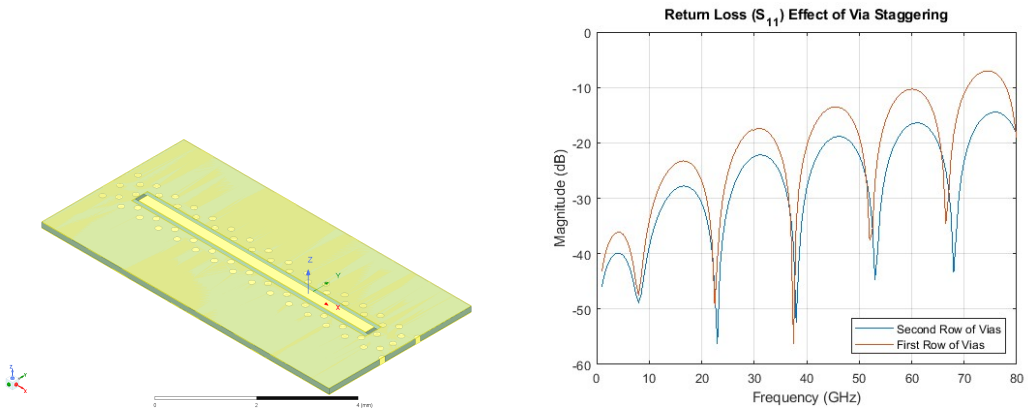


Figure 3.8: RL (S_{11}) Effect of Port Dimensions

ficient. Other rows increase the simulation and manufacturing time without adding noteworthy improvements. It is clearly seen that increasing the via staggering improves the RL value by creating a more condensed short circuit wall that prevents signal leakage.



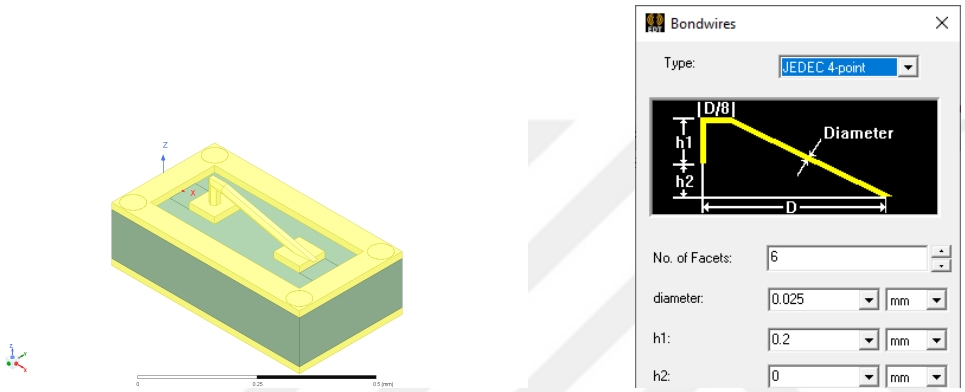
(a) 3D Model

(b) RL (S11) Effect

Figure 3.9: 3D Model and Results of Via Staggering

3.2.2 Wire-Bond Modelling

At this point, the through line and the die pad characteristics are examined. Hence, the model is prepared to be added to a wire-bond structure. There are different types within the HFSS tool and in the literature [47]. The initial trial is the standard Joint Electron Device Engineering Council (JEDEC) 4-point model given in Figure 3.10. There are two pads representing the connection point of the die and a surrounding ground via connection. The lumped port dimensions are dictated by the pad width and ground pin gap at both ends.

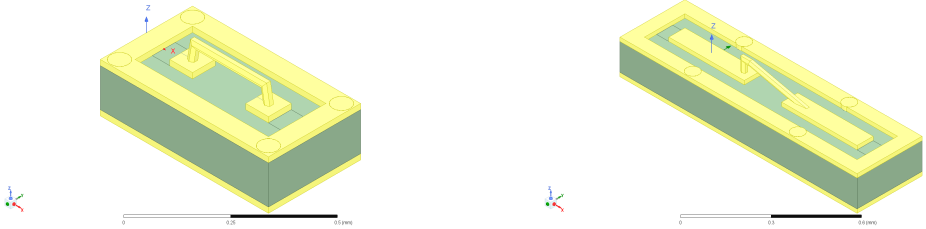


(a) 3D Model (b) 2D Parameters

Figure 3.10: JEDEC 4 Point Wire-Bond

When the standard JEDEC 4 point on top of the pad of the die result is inspected, its RL starts from -50 dB at DC but exponentially deteriorates up to -5 dB at 80 GHz. Then, two alternative approaches given in Figure 3.11 are scrutinized where one of them is changing the bending to a low profile and the other is adding the same width extensions in the beginning and end points of the same bond.

Although the three alternative cases are depicted very differently from each other, RL results are similar, as shown in Figure 3.12. After seeing a minimal effect of the bond shape, it is decided to continue with the robust one, which is JEDEC 4 point, because the bonding machines and operators are accustomed to this type.



(a) Low Profile Bond

(b) Extended JEDEC4

Figure 3.11: Two Different Approaches for Bonds

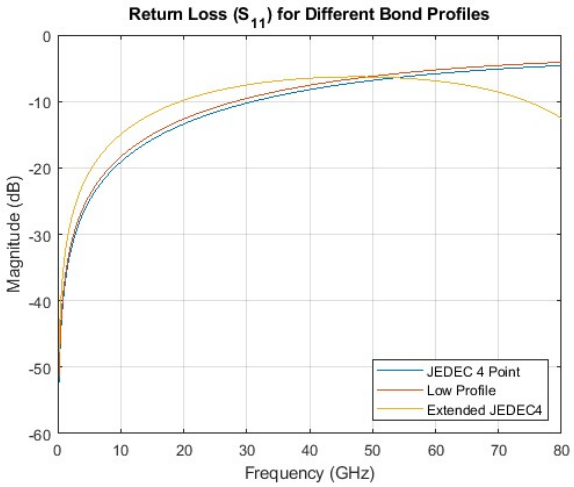
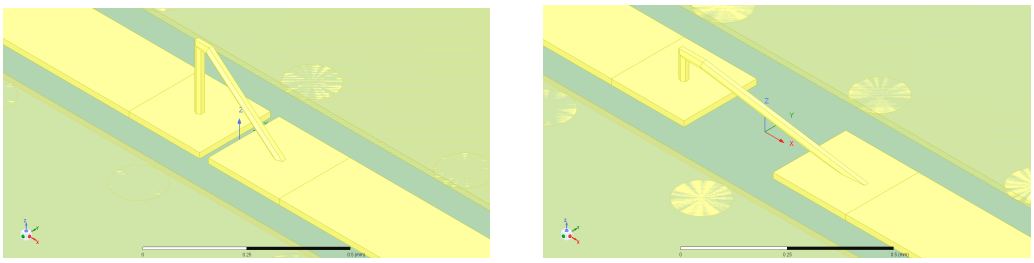


Figure 3.12: RL S_{11} for Different Bond Profiles

Since these bond wires are manufactured in certain diameters, two main design parameters are height and length/distance of the interconnection. Figure 3.13 shows the height change in the model and the change of gap between two pads.

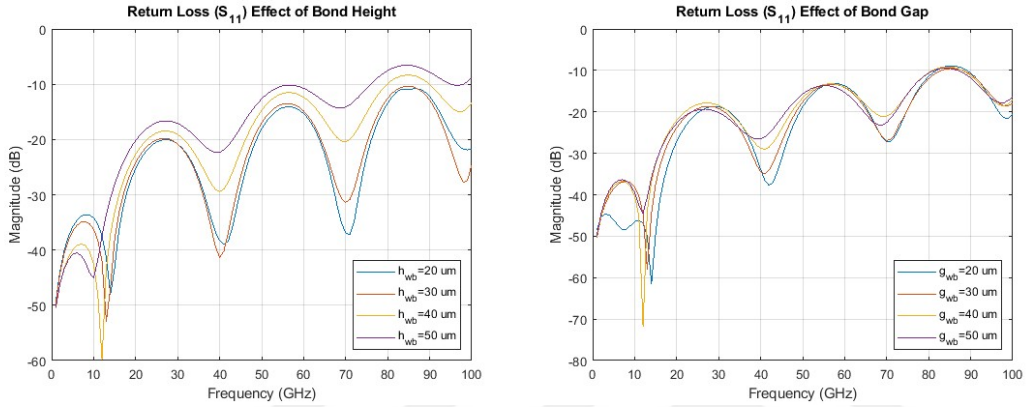


(a) Bond Height Change

(b) Bond Gap Change

Figure 3.13: Height and Gap Parameters of the Bond

The effect of the height and gap on the RL is given in Figure 3.14. There is an inverse relation between bond height and RL where the height increment from 20 to 30 μm results in 5 dB worsening in RL. When the height is further increased by another 10 μm, then the amount of change in the RL is rapidly increased up to 10 dB, concluding the bond height should be kept minimum according to the manufacturing limits. The bond gap has a similar characteristic, where the first increment of the gap changes RL minimally and further increases the gap, which results in detrimental effects on RL. Hence, both of these dimensions should be minimized.



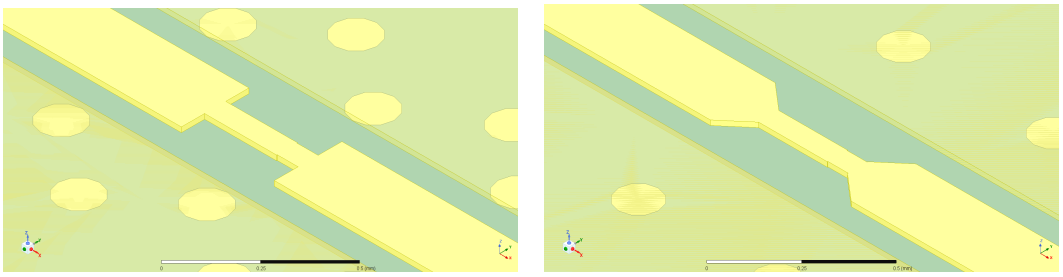
(a) Effect of Bond Height

(b) Effect of Bond Gap

Figure 3.14: Effect of Height and Gap Parameters of the Bond

After completing the necessary improvements, including bond parameters, the next stage is to study the effect of tapering. Since the through signal line width (244 μm) is larger than the die pad width (72 μm), there should be a tapering section between these two sides. To understand the reflection concept, a direct transition between these two different widths is attempted. Also, a gradual triangular tapering between these two widths is modeled for comparison as given in Figure 3.15. In the beginning, this change is done within a 100 μm length.

These two cases, namely direct transition and short triangular tapering, are compared in terms of RL as seen in Figure 3.16. Due to the deterioration in the RL, this model is reconsidered in two aspects. This might be caused by the disruption in the coplanar structure or non-attenuated evanescent modes in a short line segment. Increasing the length of the narrow section makes the results even worse, which can be sourced from



(a) Direct Transition Between Different Widths (b) Short Tapering in a Short Line Section

Figure 3.15: Sharp and Smooth Taperings in the Same Length

more reflections happening in the transition region. The addition of a closer ground plane model for the narrow section causes resonances above -10 dB RL in the wide band. Hence, it is concluded that the wire-bond pad on the PCB should be larger than the die pad dimensions.

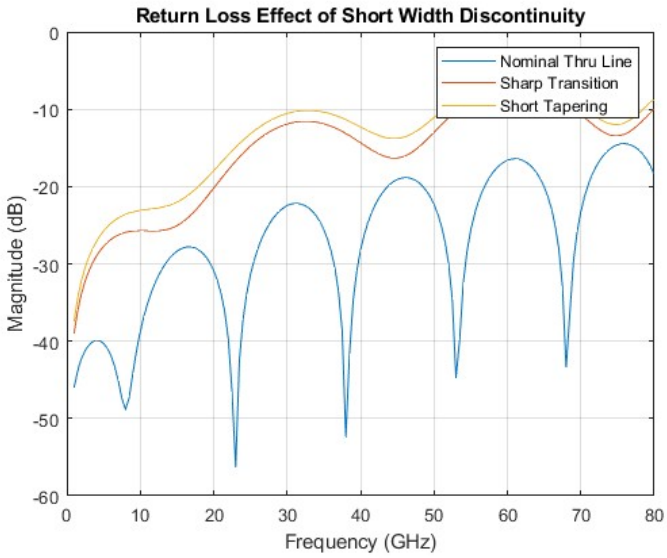
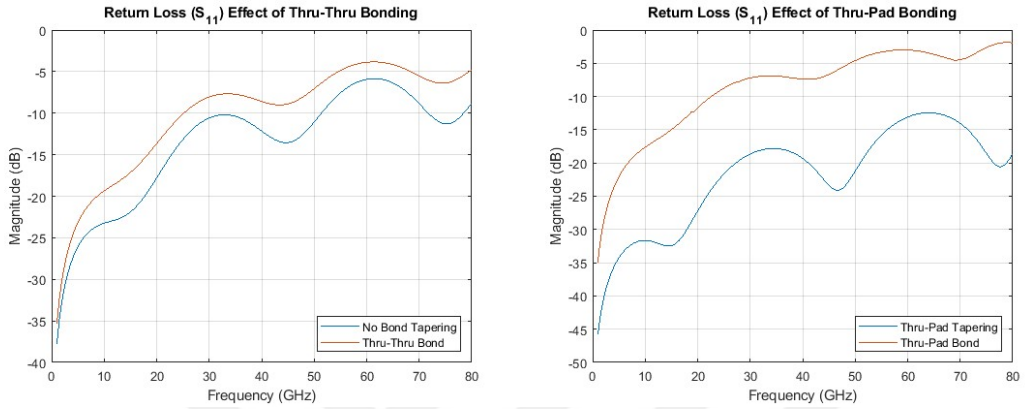


Figure 3.16: RL Effect of Short Width Discontinuity

Later, the bond and the tapering model are injected into the PCB model. The pioneer simulation is made between two through TLs. Then, the halved model is taken into account, and ground pads are connected to the PCB using direct planes. The through-through bonding case is compared with the previous no-bonding case, and results are given in Figure 3.17. It is seen that even a single bond structure can strongly deflect

incoming signals, and RL gets worse. The through-pad bonding case is compared with the previous through-pad tapering case, and results are given in the same figure. Again, the addition of a bond instead of tapering resulted in worse RL values. Both of these are expected since the bond has a diameter of 25 μm, which is much narrower than the thru line and tapering line. Since the ratio of discontinuity is high, more reflection is occurred.



(a) Effect of Through-Through Bonding

(b) Effect of Through-Pad Bonding

Figure 3.17: RL Effects of Through-Through and Through-Pad Bonding

Building on the previous information about single RF bonds, there is a necessity for ground bonding in the actual application source from the GND-RF-GND nature of the die pads. There are three distinct bonds: the middle one is a signal, and the two sides are the return path. One of the design parameters is the number of bonds between each pair. Three different cases, including single RF bonding, ground-signal-ground (GSG) bonding, and doubled GSG bonding, are compared in terms of reflection as shown in Figure 3.18. At the first instant, some undesired resonances were seen, but they were just convergence problems. When these three cases are investigated, the best RL is achieved for single RF bonding between through lines, which is expected. Among two different through-pad bondings, the double GSG bonds case is better than the single GSG bonds case, which also likely relies on the previous discussion about the number of bonds between two lines.

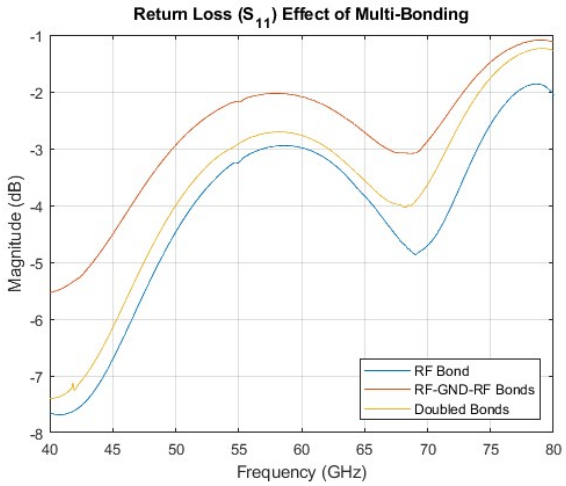


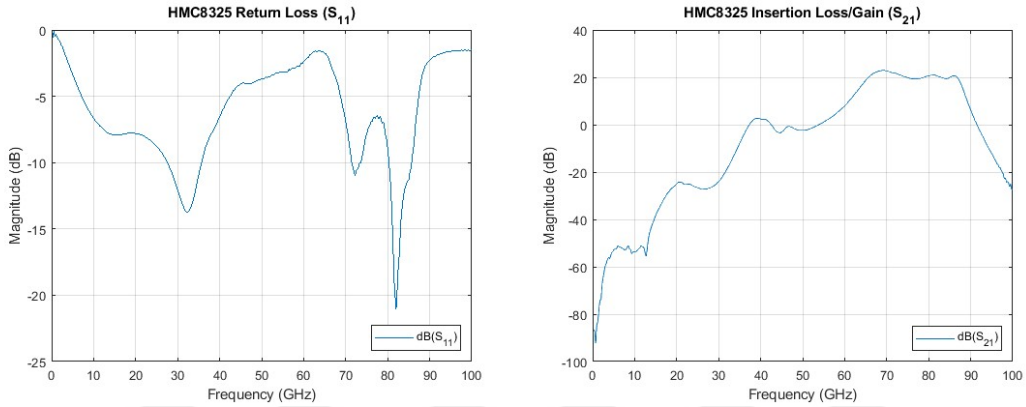
Figure 3.18: RL (S_{11}) Effect of Multi-Bonding

3.2.3 Compensation Structures: Grooving and Multi-section

As seen in the wire-bond modeling section, these interconnections distort the RL of the design even if they are chosen as shorter, with a lower profile and maximum number of bonds. According to the frequency behavior of interconnection, the 50 Ω impedance matching is disturbed between the die and PCB. It is partly compensated by creating a cavity within the PCB and placing the die inside, which is called grooving. The die has 50 μm in height, whereas the first PCB layer has 127 μm. Depending on the process, there would be 20-30 μm of silver epoxy to glue the die in both mechanical (resilience, thermal) and electrical (grounding). There is still a 60-70 μm height to be used for bending or twisting the bond profile. Since there are different ending types, such as ball and wedge, this height can be used to minimize the bond length further.

Before investigating the grooving mechanism, it is necessary to know the characteristic impedance of die pads. Also, the TL width along the die surface should be found with HFSS Q2D modeling. The die signal pad is a 72 μm width and 5 μm height rectangle on top of a 50 μm height and 999 μm width Gallium Arsenide (GaAs). HMC8325 dictates this die substrate material has a relative permittivity of 13.1, which is significantly high compared to PCB dielectrics. Also, two ground pads have 58 μm edge-to-edge distance to the signal pad. By using these values, the Q2D resulted in a

33 Ω characteristic impedance at the E-band for the die RF pad interacted with ground pads. This 33 Ω characteristic impedance is expected by examining the RL values of the die given in Figure 3.19. At the 77 GHz frequency band, the die has a -6.685 dB S_{11} value, which corresponds to 0.215 in linear. Since the RL is defined as shown in Equation (3.1), the value of Z_L should be 32.336 or 77.313 Ω for a $Z_0 = 50\ \Omega$.



(a) RL S_{11} (b) IL/Gain S_{21}

Figure 3.19: HMC8325 S Parameters

$$RL = 10\log_{10}|\Gamma_L| = 10\log_{10}\left|\frac{Z_L - Z_0}{Z_L + Z_0}\right| \tag{3.1}$$

If the die image under the microscope is reevaluated, it can be seen that the signal follows a microstrip path instead of a coplanar waveguide. Hence, a microstrip Q2D is constructed like Figure 3.20, and the required through TL width is numerically found as 18 μm.

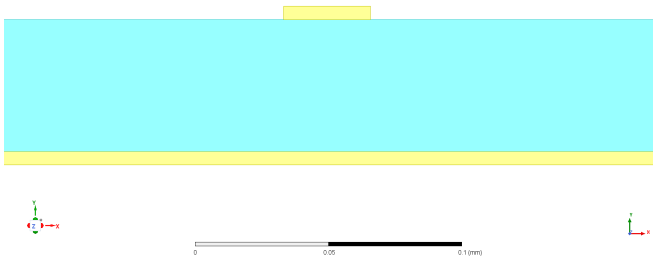


Figure 3.20: Q2D Model for Microstrip Line on Die

Once these necessary dimensions are gathered, a cavity is opened in the middle of the PCB, as shown in Figure 3.21. The initial attempt is dependent on the manufacturing limits within the company. Without violating design rule checking, drilling a minimum of five mils away from the edge of the PCB is allowed. This process became possible with the help of laser-cutting technology because mechanical drill bits could not achieve these lower values. In case of need, the cavity depth, PCB proximity, and lateral shift are also parameterized.

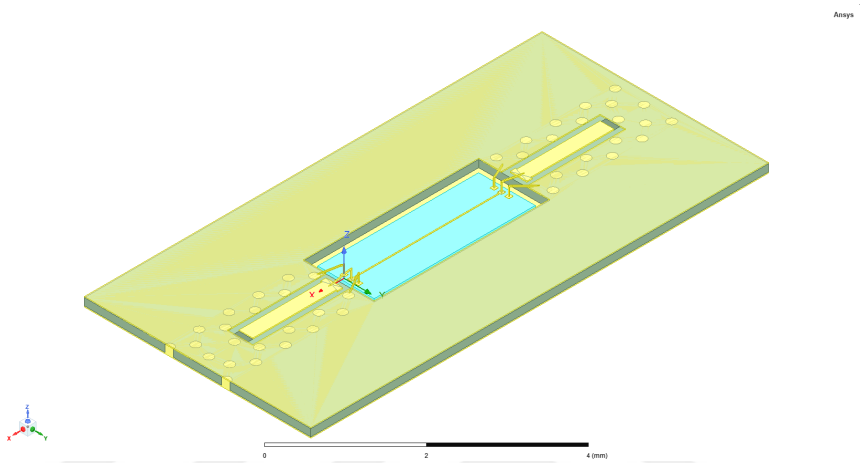
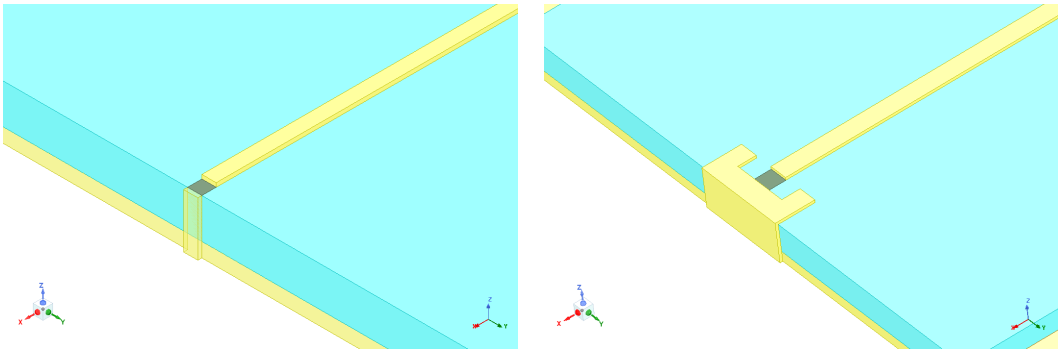


Figure 3.21: HFSS Initial Model for Die in PCB Cavity

The port definition is well-studied for the PCB side, but it is not directly applicable to the die side. Even if the GSG pads are adjacent to each other, the through TL is modeled as a microstrip. Since the halved model is used, there should be a lumped port at the end of this GaAs line. There are several options for connecting the RF and GND with a port. The first one is making a vertical rod extension as depicted in Figure 3.22 whose width is die line width and height is die height. The other option is to expand the ground plane in both vertical and horizontal directions. The ground plane of the port on the die is modeled in the launcher form similar to the PCB port where GND surrounds the port from all three directions.

These models are compared in terms of reflection as shown in Figure 3.23. It is seen that the launch port RL is 5 dB better than the rod port, and it overlaps more with the previous models.



(a) Rod Port (b) Launch Port

Figure 3.22: HFSS Half Model with Die Ports

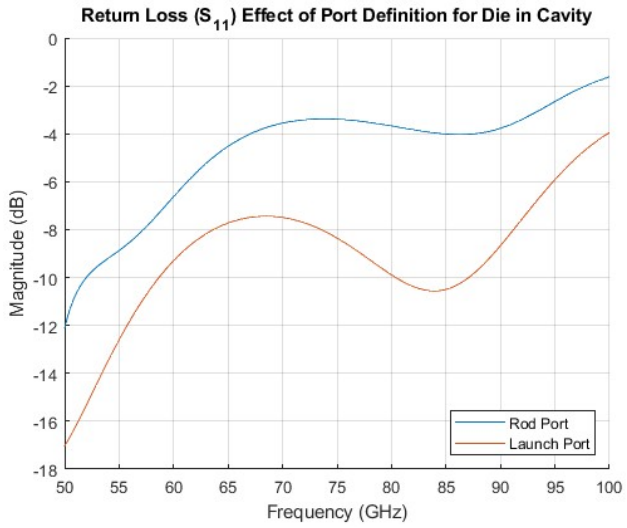
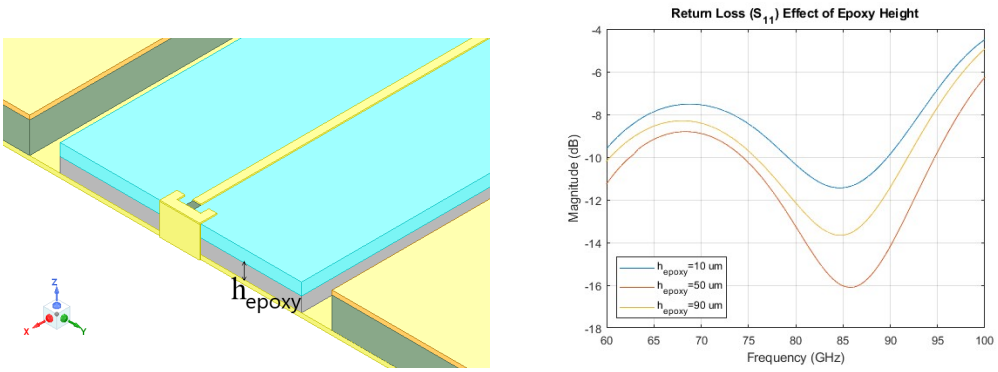


Figure 3.23: Return Loss (S11) Effect of Die Port Definition

In the previous model, the die was attached to the bottom of the substrate layer. However, there must be a binder between the die and PCB during manufacturing. The cavity depth or height difference is dependent on this adhesive-conducting silver epoxy [48]. It is a reliable and robust technique to glue the die onto a PCB cavity surface. The epoxy modeled in 3.24 is advantageous for height balancing between the die and PCB, although there is not any expected thermal concern. By inserting the epoxy, results are changing where the RL is improved until reaching an optimum point for the height balance between PCB and die.



(a) 3D Model

(b) RL (S_{11}) Effect

Figure 3.24: 3D Model and Results of Epoxy Height

This section concludes that sensitively drilled cavities and PCB finishing are necessary. The chosen dielectric substrate is RO3003 with low tan δ of 0.001, and the SR between two layers is selected as 0.4 μm, namely rolled copper. Also, a plain gold finish on top of the copper is preferred because of the IL of Ni and Pd in the ENEPIG. The first layer of RO3003 substrate is etched by 127 μm in-depth, and there is a five mils gap between the die and cavity edges to prevent cracking in the die placement process. The die is placed into this cavity by using epoxy of 30 μm height to avoid overflow during manufacturing. Since the increasing number of bonds provides improved RL and IL, the interconnection type is chosen as the thickest version, namely the three mil ribbon. The beginning and end points of the interconnection are picked as wedge type instead of ball ending to achieve a flatter incline profile. Hence, these properties define the boundaries of the uncompensated design.

The overall model is built by combining all the previous steps, including proper port definition, distribution of vias, through lines, grooving, interconnection, and matching. The parametric sweep or optimization on a complete 3D model at this frequency takes a significantly long time, and the design method is not robust and repeatable. It has been decided that the cascading of small sections can be beneficial. Each section (pad, bond, matching sub-elements) is first simulated in Q2D, and then W-element models are created. When the cascaded 2D design satisfies the specifications, 3D blocks are introduced, and differences are studied. By doing so, simulation time is decreased significantly, and changes are forecasted.

3.3 Uncompensated LNA PCB Measurements

After finishing through-line measurements, an uncompensated PCB design is manufactured. When components are soldered on the PCB, the advised flowchart is used as a baseline. The HMC8325 datasheet recommends bypassing all supply connections with adequate bypassing capacitors. Also, it is advised to use single-layer chip capacitors with a very high self-resonant frequency near the HMC8325 chip. Typically, 120 pF chip capacitors are suggested, followed by 0.01 µF and 4.7 µF surface-mount capacitors. Supply lines can be combined into single drain and single gate bias sources to minimize the number of external components and simplify power supply routing. The recommended four-channel single power supply source is 3 V. Alternatively, one can use 2 V and 4 V power supply sources for $1^{st} - 2^{nd}$ and $3^{rd} - 4^{th}$ drain pins, respectively. The HMC8325 employs several amplifier stages, all using depletion mode transistors. The bias sequence explained in Section 2.1.4 is recommended to prevent damage during power-up.

The uncompensated PCB design with a sensitively opened cavity is given in Figure 3.25. On the left-hand side, PCB land patterns are shown, while the right-hand side includes DC circuit components, including voltage regulator, inverter, switch, potentiometer, op-amp, and buffer.

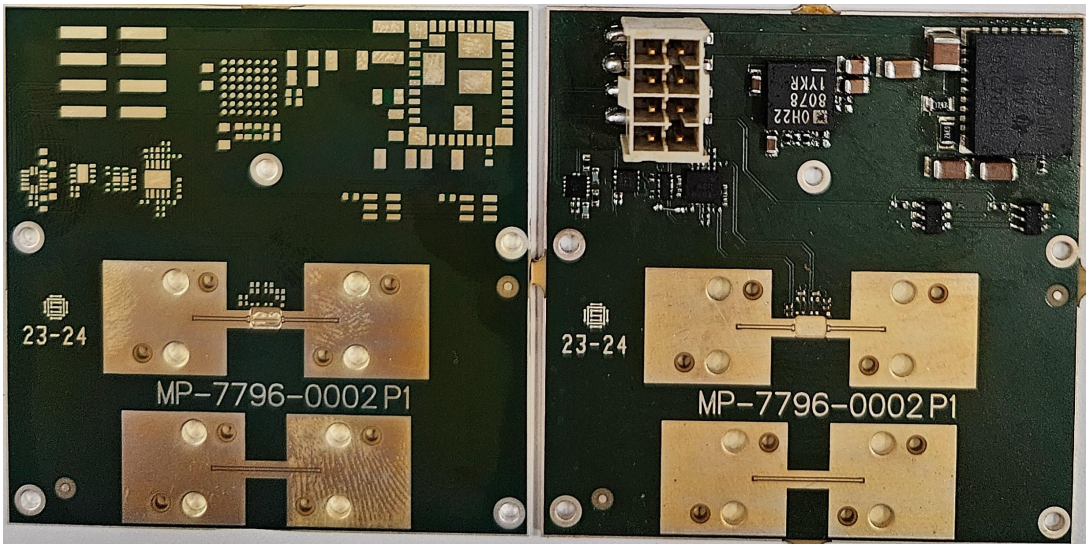


Figure 3.25: Uncompensated PCB Design with Cavity and DC Circuitry

An initial trial of 3 mil (76 μm) ribbon bonding in RF connections and one mil (25.4 μm) wire bonding is done and investigated under the microscope as seen in Figure 3.26.

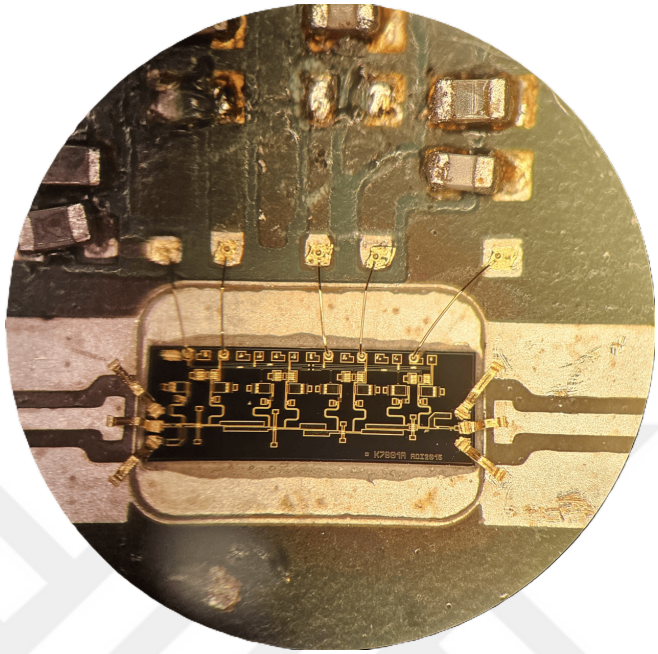


Figure 3.26: Ribbon and Wire Bondings Under Microscope

Then, the RF performance is measured in the setup given in Figure 3.27. Measurements are taken in continuous wave (CW) mode. Since the LNA has a low power consumption, it does not require any mechanical or liquid cooling structure. The transceiver that creates the necessary RF input signal works with 5 V (760 mA), and it has to be cooled laterally by a standard 24 V fan. This transceiver PCB is controlled by a SUB-20 card via a MATLAB code, which changes the frequency and internal attenuation. Then, this RF signal is transferred to the LNA PCB by a 1 mm diameter SMA cable. The output signal of the LNA is transferred through a variable attenuator. The signal analyzer PXA works up to 50 GHz frequency, and its band is extended by using a W-bant external mixer module. When using this setup, proper analyzer settings should be done by opening the corrections and importing the conversion loss table of the mixer. The resolution BW is taken as 10 kHz, and the frequency span is settled at 100 MHz to see the generated signal. Also, a broader span is investigated to check whether there are any parametric oscillations or not.

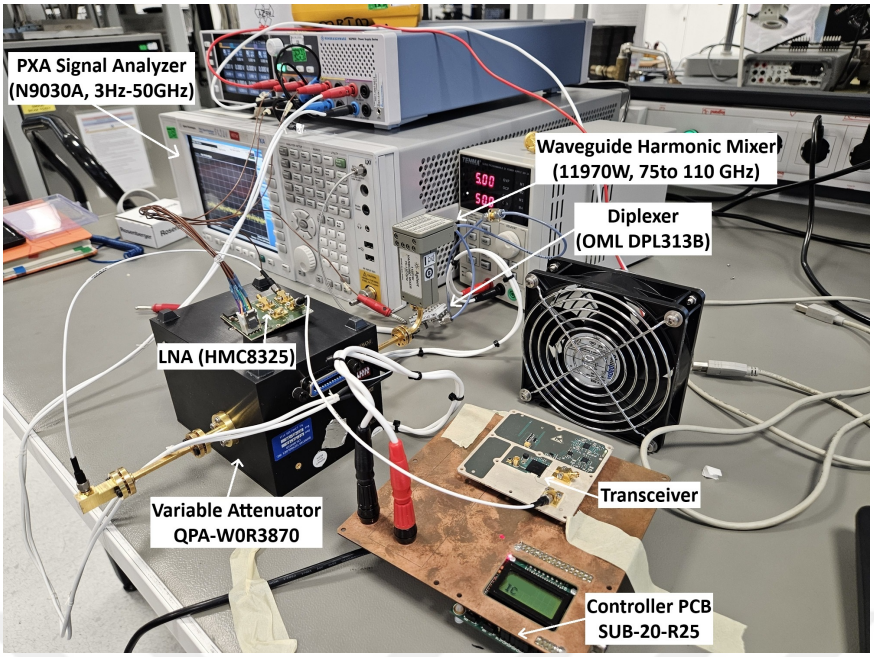


Figure 3.27: Measurement Setup

An exemplary measurement result is given in Figure 3.28. The data is taken at 77 GHz and read as approximately -20 dBm. When the LNA is taken out of the RF strip and the through line is connected, this value is -41 dBm. Hence, the LNA structure provides a 21 dB gain.

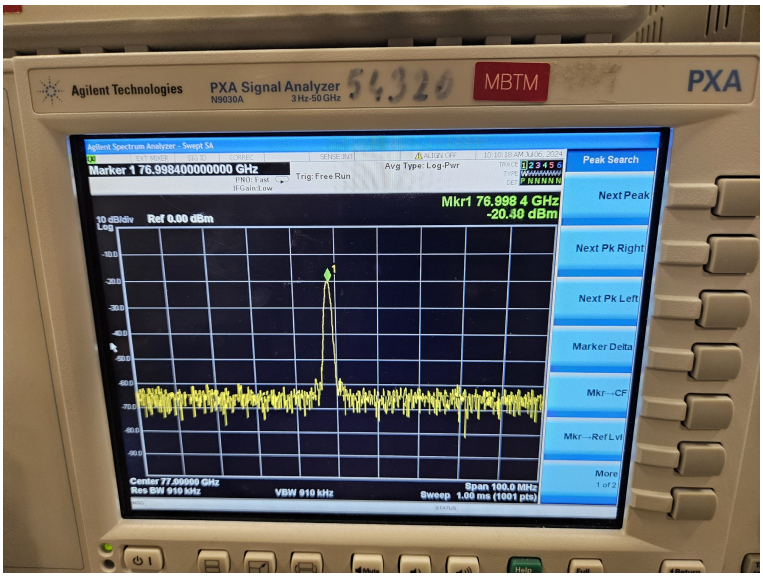


Figure 3.28: Signal Analyzer Result

Since the transceiver does not have an automatic frequency sweep feature, the remaining data is taken manually by changing the frequency and internal attenuation. The gain variation for an input power sweep is done for distinct frequencies as in Figure 3.29.

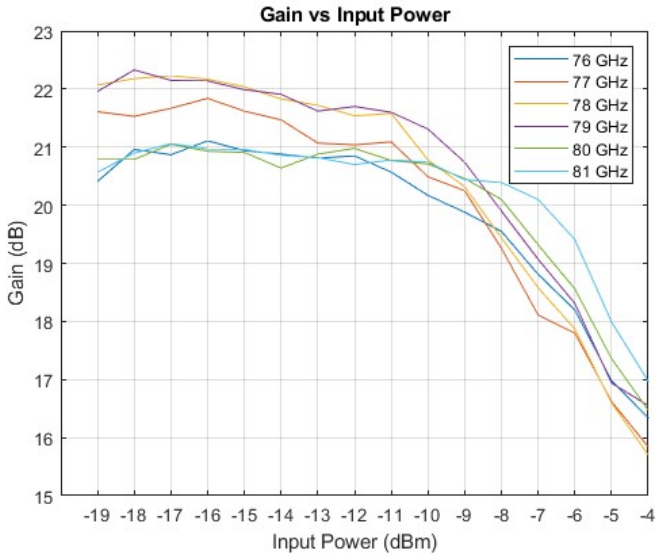


Figure 3.29: Measured Gain vs Input Power for the Uncompensated Design

These values can also be interpreted as a frequency sweep for constant power levels as shown in Figure 3.30.

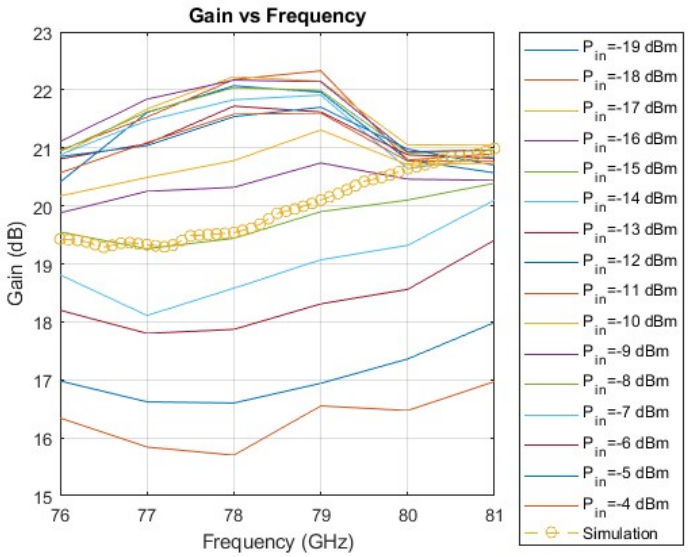


Figure 3.30: Measured Gain vs Frequency for the Uncompensated Design

A smart noise source at E-band is required to measure the NF of the design. Thanks to the demo setup and FS-SNS110 device provided by Rohde Schwarz, 6-point data is taken within the 76-81 GHz band as shown in Figure 3.31.

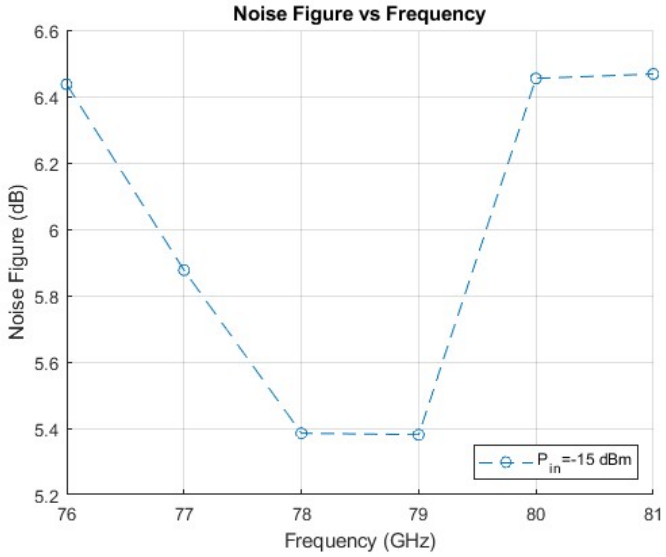


Figure 3.31: Measured NF for the Uncompensated Design

CHAPTER 4

MATCHING SECTION DESIGN AND OPTIMIZATION

This chapter emphasizes a systematic approach to design optimization and verification to guarantee accuracy and efficiency. Through Q2D and HFSS studies, Section 4.1 investigates the use of cascaded block approaches, providing an in-depth understanding of the performance of the system at various abstraction levels. To mitigate performance degradations brought on by interconnections, a compensation model created utilizing Particle Swarm Optimization (PSO) is presented in Section 4.2. The measurement findings are finally shown in Section 4.3, which provides experimental confirmation of the suggested design process and its efficiency in reaching the targeted performance parameters.

4.1 2D/3D Hybrid Model

After creating the uncompensated model consisting of die, interconnection, and through lines, a matching circuit on top of the PCB must be designed, which compensates for the RL degradations. An exemplary compensation network is depicted in Figure 4.1. In the low-frequency bands, the overall design can be optimized by defining variable width and length parameters for each matching section. However, in the EHF band, this procedure requires significantly longer simulation time and creates a considerable processing load. Instead, a hybrid model is proposed in this thesis, which consists of W-element models of capacitive and inductive matching sections as shown in Figure 4.2. It also includes the mutual capacitance between capacitive (wide) sections and asymmetric discontinuity models at each junction point. By doing so, computational work is lightened, and simulation time decreases dramatically.

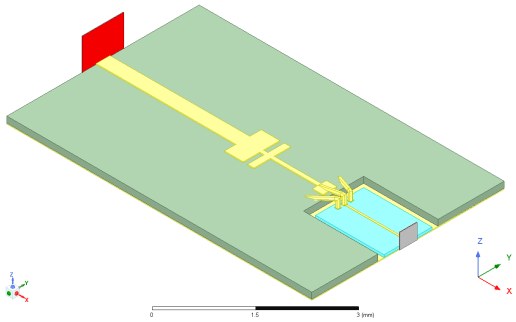


Figure 4.1: Exemplary 3D Matching Design

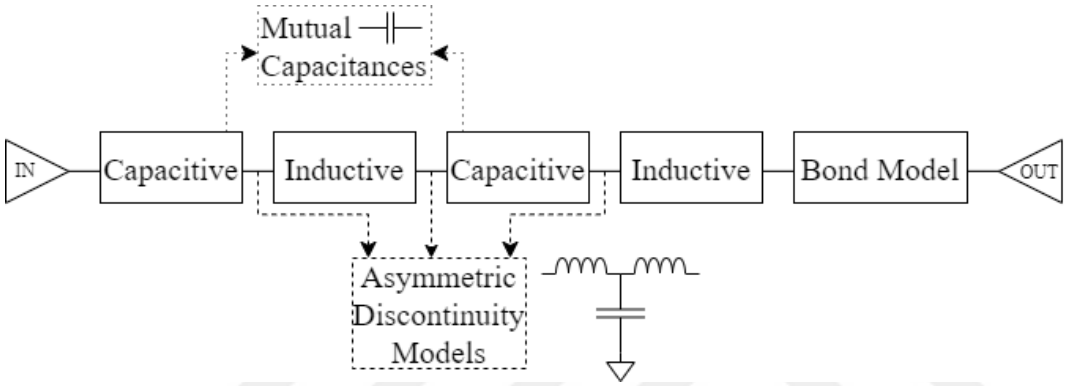
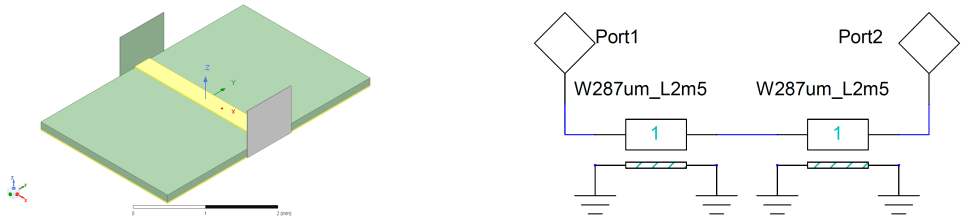


Figure 4.2: Proposed Hybrid Model for Optimization

Beyond the RLGC and HSPICE models, Ansys Circuit has a W-element option, which creates the line parameters per unit length through the frequency band. The W-element utilizes an advanced TL simulation technique that is exceptionally fast, accurate, and reliable. HSPICE can model a variety of TLs using the W-element, which is based on distributed RLGC matrices [49]. This method is highly versatile and suitable for most interconnect systems because it can represent any number of coupled interconnects and manage significant frequency dependencies. The inputs for each W-element model include matrices for R_0 (DC resistance), L_0 (DC inductance), G_0 (DC shunt conductance), C_0 (DC capacitance), R_s (skin-effect resistance), and G_d (dielectric-loss conductance).

After creating the necessary W-element models for building blocks, it is concluded that the wave port with de-embedding should be continued in the thesis for coherence in the cascading process. An HFSS model of the through microstrip line is created

as shown in Figure 4.3 obeying the wave port extension coefficients. This HFSS model is used to compare results with the cascaded W-element model given in the same figure. The first step is the connection of two through lines, and their widths are provided by 287 μm, and lengths are 2.5 mm.



(a) Through Line with Wave Ports

(b) W-Element Model of Through Lines

Figure 4.3: Model Comparison for Through Line

The cascaded W-element and the complete HFSS model results are compared in Figure 4.4. The agreement between the 2D and 3D models is acceptable. Although the resonant depth values differ from each other, the resonance frequencies are correlated. Since the W-element model is extracted from Q2D analysis and there is only excitation signal assignment, the wave port definition in the 3D model still affects the RL values. Also, the RL result of the W-element model reaches the - 70 dB levels, which is practically impossible even for the through line.

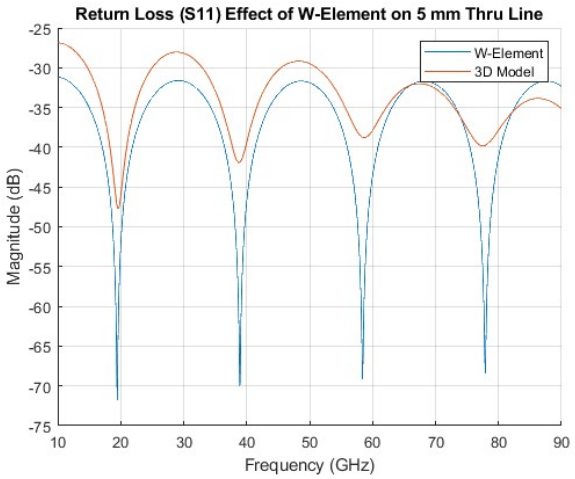


Figure 4.4: RL (S11) Effect of W-Element on 5 mm Through line

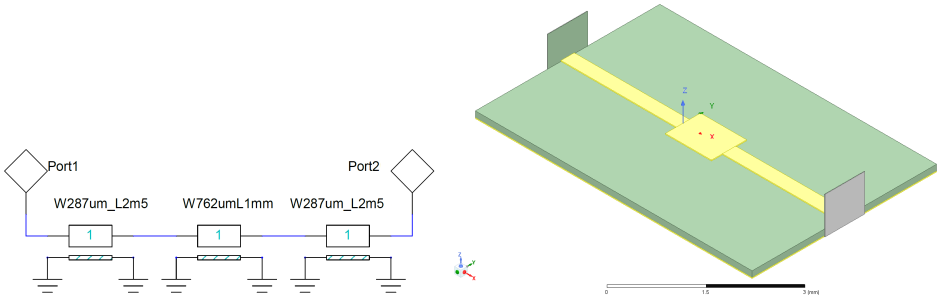
After completing the cascaded through line modeling, capacitive (wide) and inductive (narrow) distributed TL parts should be modeled in W-element. Creating a higher impedance difference between L and C sections, the required number of sections can be decreased. Since the narrowest line can be manufactured with a width of 3 mils (76.2 μm), the wider line is chosen as ten times the narrower one, that is, 30 mils (762 μm). Further increase of this upper limit occupies larger spaces than the die in the transverse direction, which is not desired because these final LNA products are used in parallel within a multiple-channel structure. Hence, the narrow and wide lines are modeled in Q2D as shown in Figure 4.5, and characteristic impedances of matching sections are found. The inductive one has 92.9 Ω while the capacitive one has 24 Ω impedance.



(a) Narrow (76 μm) Line (b) Wide (762 μm) Line

Figure 4.5: Q2D Models of Narrow and Wide Line Sections

By using the previous Q2D information, a capacitive section having 762 μm width and 1 mm length is inserted between two through lines as shown in Figure 4.6. One distinct resonance is seen around 90 GHz. The red curve in Figure 4.9 has a frequency shift caused by the interactions occurring at the impedance discontinuities.



(a) Cascaded W-Element Model (b) HFSS Model

Figure 4.6: Models for Through and 1 mm Capacitive Lines

The reason behind the frequency shift is studied through the discontinuity principle given in Figure 4.7. When the impedance suddenly changes, and the line width decreases, some portion of the electric field is concentrated in a narrower region while another portion is scattered through the edges. This effect can be modeled as a shunt capacitor and two series inductors in Tee type. These values can be analytically calculated with the following Equations (4.1), (4.2) and (4.3) by substituting the values [50].

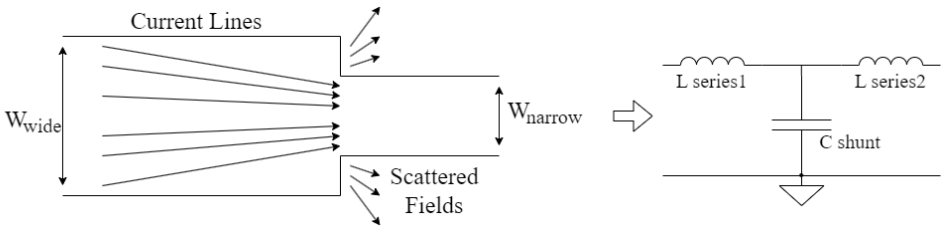


Figure 4.7: Microstrip Discontinuity of Change in Width

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2}\sqrt{(\frac{1}{1 + 12\frac{h}{W}})} \tag{4.1}$$

$$C_{shunt} = \frac{\epsilon_{eff}(W_{wide} - W_{narrow})}{c_0 Z_{wide} Z_{narrow}} \tag{4.2}$$

$$L_{series} = \frac{Z_{narrow} - Z_{wide}}{2c_0} \tag{4.3}$$

Since there are two identical junction points in Figure 4.6 between 762 μm and 287 μm width lines, they can be modeled as two Tee-type lumped models. The impedance of the wider (capacitive) section is found as 24 Ω. When the corresponding 3.3 fF capacitors and 43.3 nH inductors are connected as in Figure 4.8, similar results are obtained with the HFSS model. Hence, the red curve that represents plain W-element model shifts, and the yellow curve in Figure 4.9 is obtained.

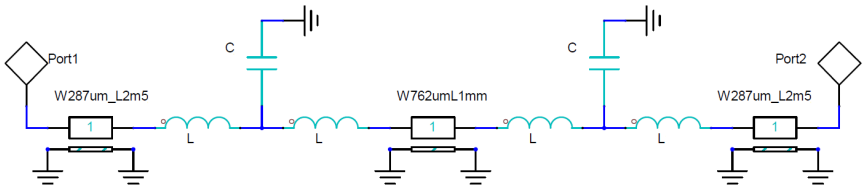


Figure 4.8: Updated W-Element Model of Through-Capacitive Lines

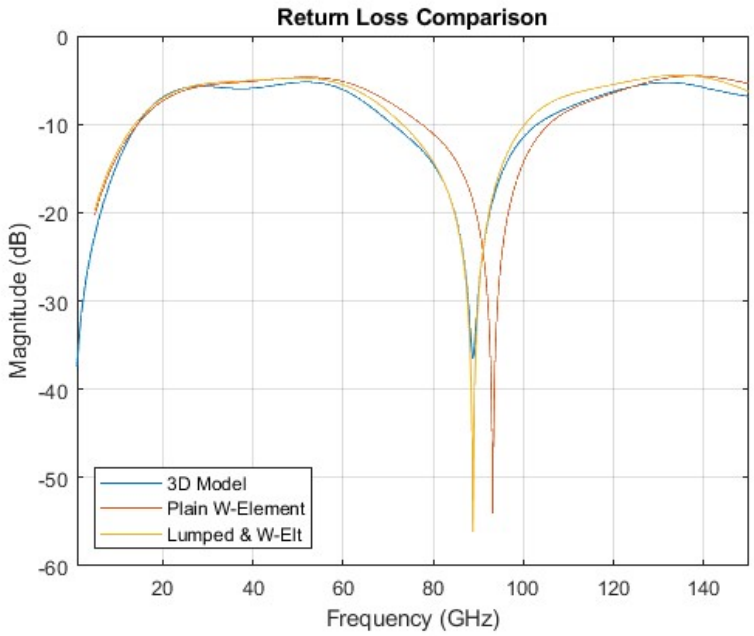
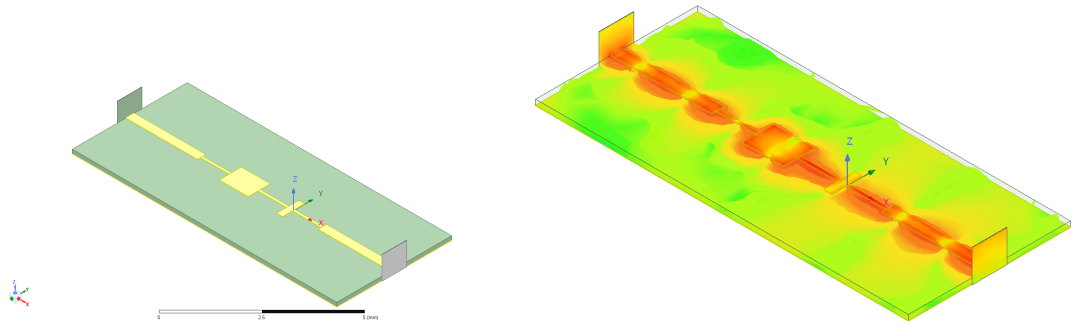


Figure 4.9: RL ($|S_{11}|$) Effect of W-Element on 1 mm Capacitive Line

In the previous comparison, lengths of the matching blocks were identical resulting a symmetric discontinuity model. However, the value of the series inductance in the discontinuity depends on the size of the following stages. If Figure 4.10 is investigated, it can be seen that the field distributions in the first and second capacitive (wide) sections are different from each other. The field cannot reach its maximum value in a short distance; hence, the inductive behavior is more dominant even if the width ratio between L and C is the same.



(a) HFSS Model

(b) E-Field Distribution

Figure 4.10: Asymmetric Matching and Resultant Field

To find the relation between the length of the C line between L lines and the required W-element model inductor value, the 3D HFSS model given in Figure 4.11 is created. In this model, the length of through and inductive lines are kept constant while the length of the capacitive section is changed. By doing so, the field distribution on the C line changes, and the required discontinuity inductor value changes to obtain compatibility between the two models.

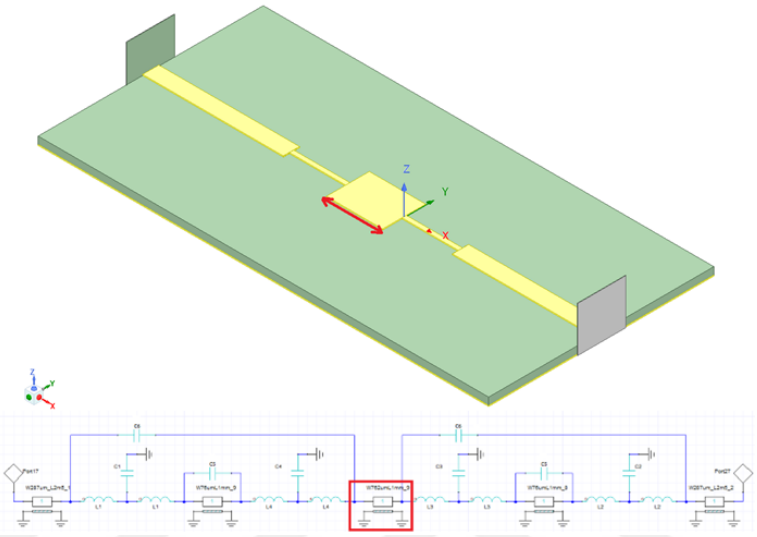


Figure 4.11: HFSS Model for Parametrization of C Line Between Ls

According to the resultant lumped inductor values, these points can be fitted on a curve as shown in Figure 4.12. Equation 4.4 summarizes the relation between the length of the C line (C_{len}) in the HFSS model and the required lumped L value (L_{disc}) in the discontinuity model. For values in this interval, the inductance can be interpolated, and for other values, it can be extrapolated.

$$L_{disc} = \left(\frac{68}{1 + \frac{C_{len}^2}{2.56}} - 48\right) \text{nH} \tag{4.4}$$

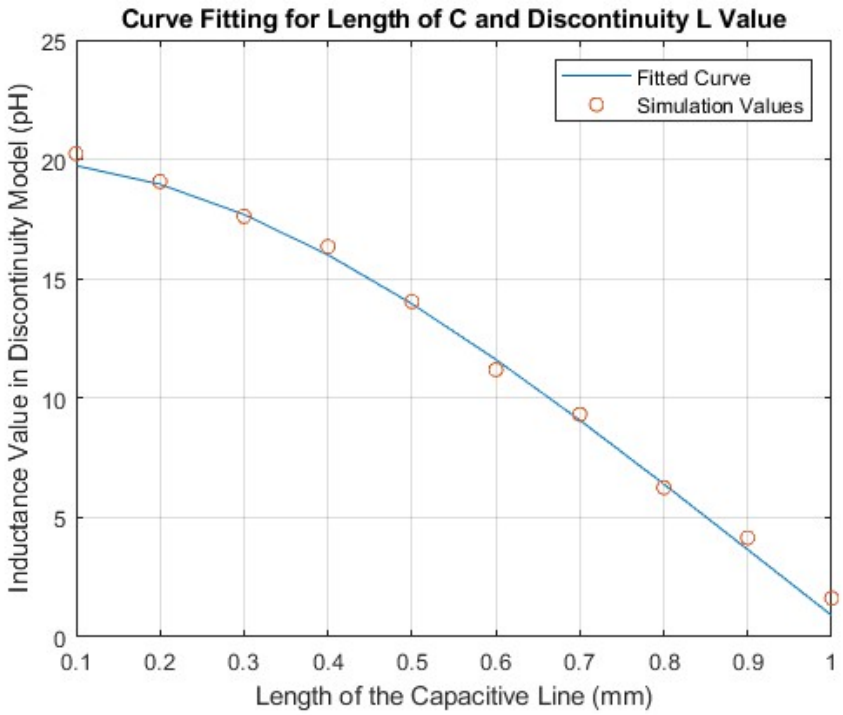


Figure 4.12: Curve Fitting for Length of C and Discontinuity L Value

Similar to the capacitive case, an inductive line with 76 μm width is modeled as in Figure 4.13 and simulated in the complete HFSS model. In addition to the L_{series} and C_{shunt} at the discontinuities, a series capacitance is included in the model to present the mutual coupling between wider sections of the line.

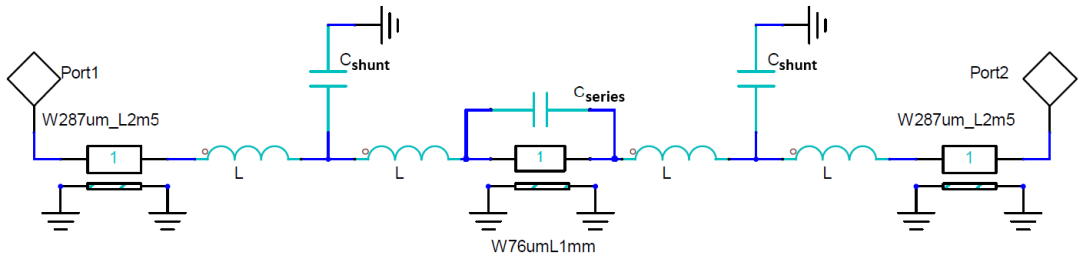
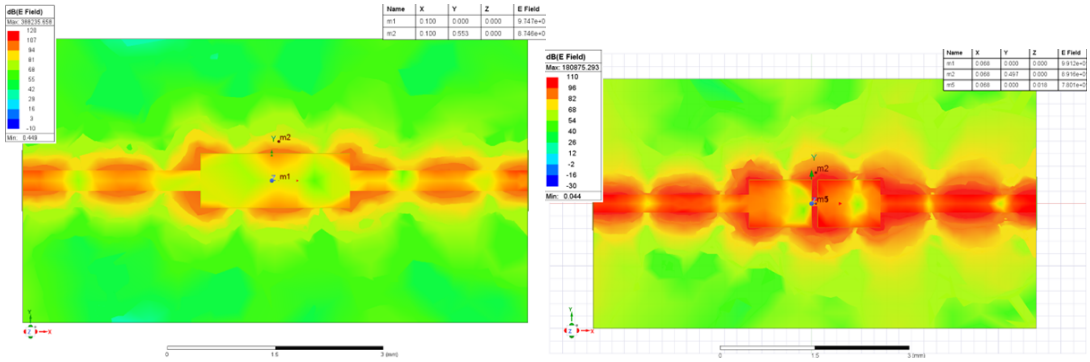


Figure 4.13: Cascaded W-Element Model of Through and 1 mm Inductive Lines

To predict the C_{series} values as a function of design variables, an HFSS model is created consisting of capacitive and inductive sections with varying widths and lengths. Figure 4.14 illustrates the increased field intensity between the wider line sections, verifying the above discussion.



(a) Fully Capacitive Model (b) C-L-C Model

Figure 4.14: Electric Field Plots for C-C and C-L-C Cases

In the literature, one study investigates the mutual coupling in coupled sub-wavelength periodic microstrip lines [51]. However, the model is examined for two TLs that are placed alongside each other, and it is not applicable to this thesis. A response surface for C_{series} is generated by simulating 27 combinations of the variable values using the sampling points 400, 510, and 630 μm for the width of one side; 720, 850, 990 μm for the other side; and 100,200 and 300 μm for the length of the narrow section. For each case, the RL of the 2D and 3D models are compared, and the C_{series} value is manually adjusted.

The resultant 3D surface is given by Figure 4.15. The right horizontal axis is the summation of widths of two wide lines after the extraction of narrow line widths. The left horizontal axis is the length of the narrow line. This equivalently shows the gap between wider lines. The vertical axis shows the required lumped capacitance in the W-element model. It is seen that similar to a parallel plate capacitor, there is a proportional solid relation between the total width and lumped capacitance value. Also, the capacitance is inversely proportional to the length of the narrow section. For the sake of completeness, the 3D surface is projected onto x-z and y-z planes as shown in Figure 4.16. The x-z projection shows the inversely proportional relation in a more detailed way, whereas y-z has a linear behavior with discrepancies.

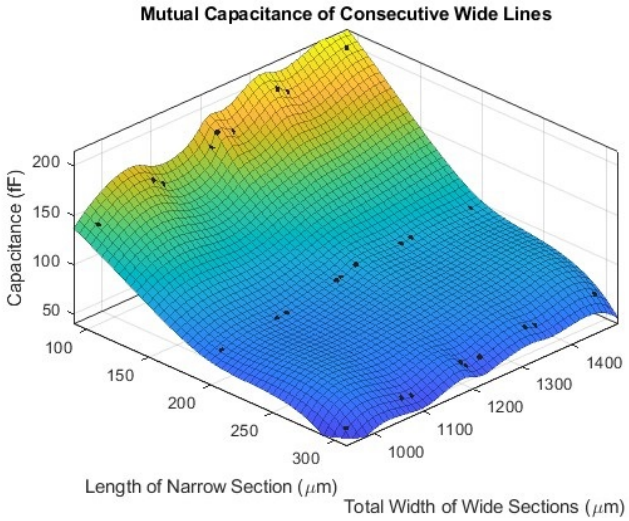
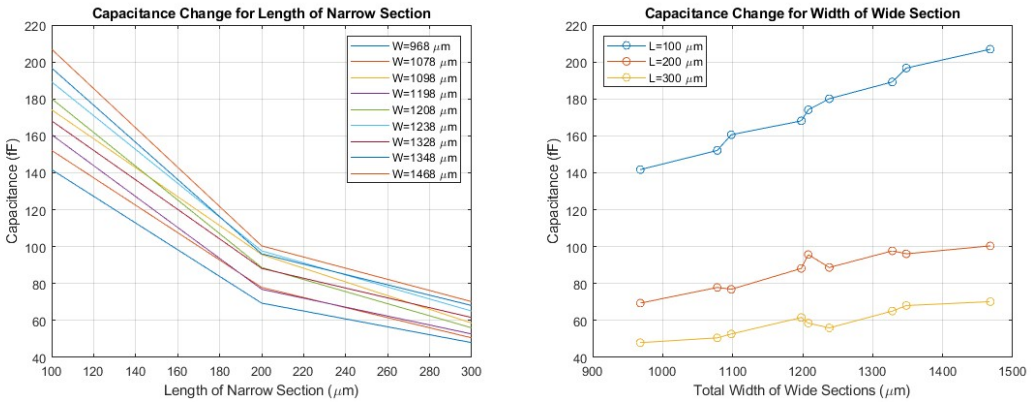


Figure 4.15: Mutual Capacitance Values of Consecutive Wide Lines



(a) X-Z Projection

(b) Y-Z Projection

Figure 4.16: Projections of the 3D Surface Result

When the red curve in Figure 4.17 is examined, the frequency shift problem is reversed with respect to the capacitance case. However, the damping of the $|S_{11}|$ values of the HFSS model is more visible for the lower frequencies. Suppose the lumped element values are recalculated for this design. In that case, the capacitance is found to be 0.35 fF, and the inductance is 71.5 nH since the impedance of the inductive section is given by 92.9 Ohm in section 3.2.5.

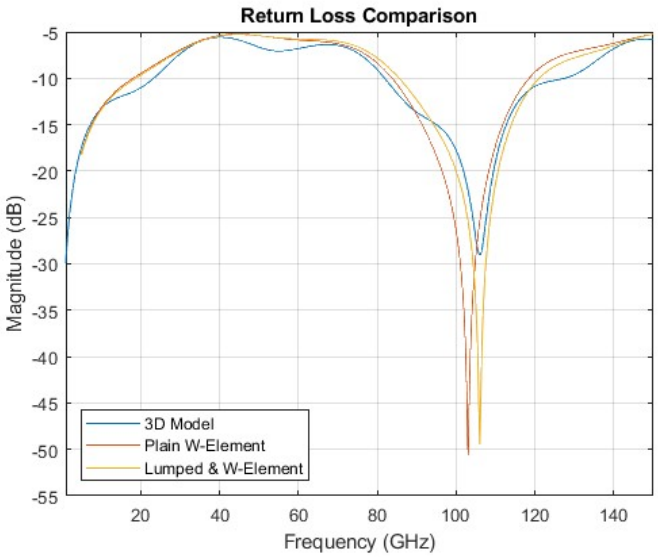


Figure 4.17: RL ($|S_{11}|$) Effect of W-Element on 1 mm Inductive Line

When the TL parts (through, capacitive, inductive) are separately simulated using Q2D, fundamental W-element blocks can be used by changing the length of each part. Not only single L or single C but also 1-2-3 stage LC structures are confirmed using both the Q2D and HFSS models. When the number of stages is increased to two, as in Figure 4.18, the mutual interactions become dominant.

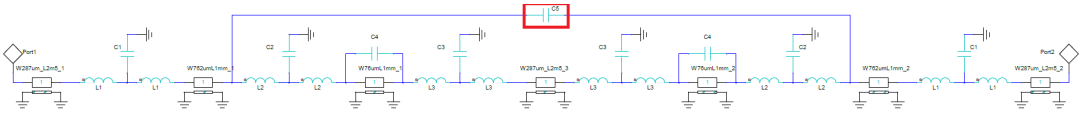


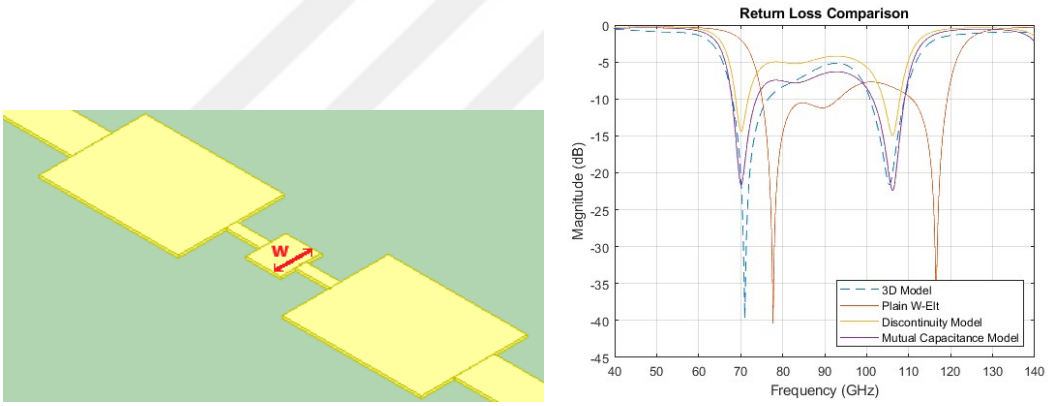
Figure 4.18: Cascaded W-Element Model of 2 Stage LC Lines

There is a changing mutual capacitance between two wide lines according to the width of the middle line section as shown in Figure 4.19. The width of the middle section is parametrized from 3 to 27 mils with 3 mil steps and the required lumped capacitor values required in W-element model are analyzed as shown in Table 4.1. When the width of the middle section is started from 3 mil, the result is the same with previous mutual capacitance between consecutive wide lines separated by 300 μm distance as expected. When the width of the middle section is increased, the weak mutual capacitance value decreases gradually because of the barrier effect.

Table 4.1: Weak Mutual Capacitance Between Far Sections

Width of Line (mils)	3	6	9	12	15	18	21	24	27
Lumped Capacitor (fF)	70.2	62.5	55.8	52.2	44.4	38.5	29.7	24.1	13.9

According to the results, the plain W-element model (orange curve) has the same characteristics up to 60 GHz and a similar waveform beyond that frequency as shown in Figure 4.19. However, the frequency shift is severe in terms of both absolute and relative change with respect to the 3D model result depicted with dashed blue line. When the discontinuity values and two dominant mutual capacitances are added to the model, the resonant frequencies of yellow line became similar to the HFSS model, but still, the RL values were considerably different. After modeling the effect of weak mutual capacitance between relatively far sections which is shown by the purple line, the degree of agreement between the outcomes derived from the 2D and 3D models is consistent, indicating that it falls within a reasonable range for the intended use.



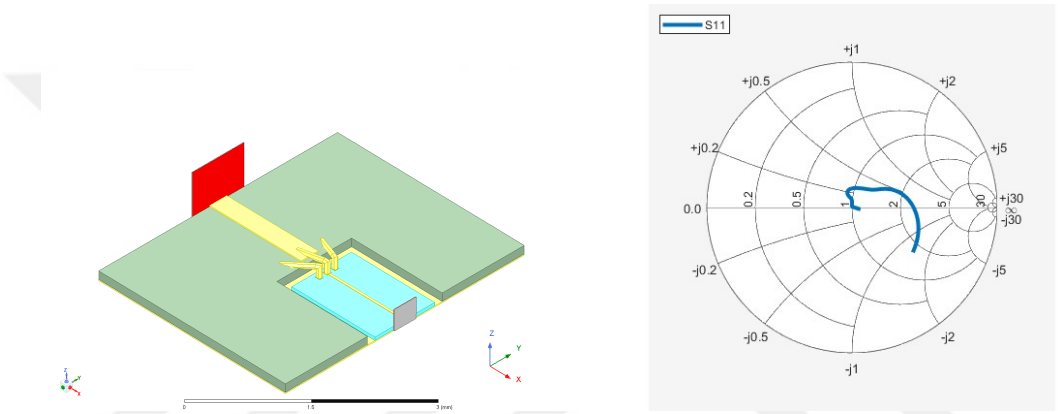
(a) HFSS Model

(b) RL ($|S_{11}|$) Comparison

Figure 4.19: 2 Stage LC Lines HFSS and W-Element Compatibility

These alignments show that the critical parameters of modeling methodologies and underlying assumptions are precise enough to produce equivalent results. As a result, any differences are probably insignificant or within acceptable bounds for the particular analysis being carried out. This validation offers assurance regarding the dependability of the simplified 2D model and its capacity to roughly represent the more intricate 3D model in the specified circumstances.

The main motivation behind the cascaded W-element method is finding a fast and optimum compensation solution for the wire-bond model and its RL on the Smith Chart given in Figure 4.20.



(a) HFSS Model of Bonded Die

(b) RL of Bonded Die

Figure 4.20: Uncompensated Model and Result

In the microelectronics domain, a bond is generally modeled as a series and constant valued lumped inductor, and each paralleling decreases this value by its portion [52]. This is attributed to the following Equation (4.5) where the length and diameters are taken in mils. At low frequencies, 39.37 mils (1 mm) length and one mil (25.4 μm) bonds are used, and 0.8 nH constant inductor value is found. However, it is valid in the sub-40 GHz frequency band. When the frequency is further increased, and pad dimensions shrink, the bond effect becomes near high resistive values and can cross over to the capacitive region depending on the proximity of the bonds and pad dimensions.

$$L_{wb} = 5.08 \cdot 10^{-3} l(\ln(4l/D) - 1) \text{ nH} \tag{4.5}$$

4.2 Low Fidelity Optimization using PSO Algorithm

The previous discussion verifies the reliability of the 2D model. When designing a specific matching circuit for a given load impedance, target RL and IL are obtained by optimizing the overall dimensions. Although there are built-in optimization algorithms in the HFSS model, the simulation time is much longer with respect to the W-element model. There are also optimization tools for Ansys circuit schematics, but they do not have the flexibility to change the width of the matching sections. Ansys Q2D has an option for exporting the RLGC parameters of these distributed sections for each frequency. This information can be imported into MATLAB and converted to S parameters. As an initial study, a single-stage matching network with minimum length is designed. In this study, the starting matching section nearest to the wire bond is an inductive (76 μm width) W-element block as shown in Figure 4.21. The complete HFSS model is illustrated in Figure 4.22.

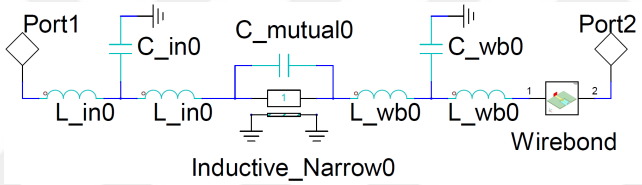


Figure 4.21: Circuit Representation of Cascaded Wire-bond and Inductance

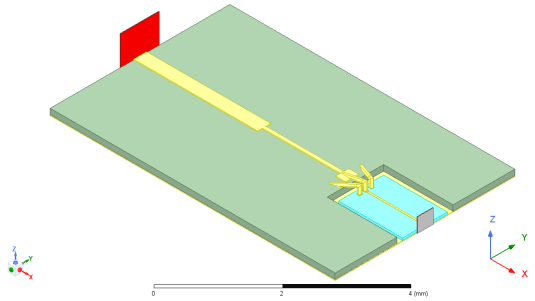


Figure 4.22: HFSS Model of Wire-bond and Inductance

In order to start the optimization process, the initial step is choosing the algorithm and its parameters. One of the simple and effective optimization technique is known as PSO. Based on position and velocity, each particle represents a possible solution in the

search space. During iterations, the algorithm modifies the position of the particle and keeps track of the best location each particle discovers along with the best position identified by the entire swarm. The velocity regulates the rate of exploration of a particle in the search space. Throughout the optimization process, it is dynamically adjusted. Particles are initialized at random at the start of the method, and these values are iteratively adjusted based on both individual and group experiences.

There are different hyper-parameters of PSO algorithm including swarm size, maximum iteration, maximum stall iteration, inertia weight, cognitive and social coefficients. The larger swarm size increases both the computational cost and the amount of search space exploration. Although they run the danger of convergent too soon, smaller swarms could converge more quickly. Hence, 10 to 50 particles are frequently enough for the majority of issues. The maximum iteration guarantees that even in the event that the algorithm fails to converge to an ideal solution, the process will be nonetheless terminated. It depends on the scale of the problem but common optimization tasks often have between 100 and 500 iterations. The stall is the number of repetitions that end without a discernible improvement. It helps to avoid squandering processing time on inactive searches. Depending on the optimizing environment, it can take values from 10 to 50.

The inertia of the particle (momentum from its prior movement), cognitive motivation to return to its personal best, and social propensity to move toward the global best all affect its velocity during each iteration. These elements are balanced using adjustable weights to guarantee a trade-off between the exploitation of known solutions and search space exploration. While a small inertia weight promotes exploitation (local search), a high inertia weight encourages exploration of the search space (global search), and it is often between 0.4 and 0.9. To move from exploration to exploitation, it can also be gradually decreased over time. An increased value for cognitive coefficient motivates the particle to explore based on its past experiences, raising the chances that it will move towards its most familiar location. A greater social coefficient value promotes the swarm convergence on the best solution by enhancing the chances of the particle moving toward the globally accepted position. These two coefficients are used as 2 as a default and they are finely tuned between 1.5 and 2 when needed.

After deciding the algorithm, design parameters of the network are established. Then, the network is splitted into nodes and each node possess clearly defined input and output ports. After the basic structure has been set up, relevant variables are assigned to their initial values, ensuring that appropriate limits are applied to each. Afterwards, PSO is employed to enhance the network efficiency after configuring these parameters. Next, the objective function is calculated and the penalty value is evaluated ensuring that the network meets all essential criteria at this point. The process concludes once the requirements are met. If that's not the case, it is returned to the PSO phase and continues refining the solution until every requirement is satisfied [53]. Additional information on the PSO approach can be found in Appendix A. At this point, an objective function should be defined to achieve the optimum solution. In this first case, it can be specified as the summation of penalties with respect to the error values (difference between instant and aimed result) of S11 as shown in Figure 4.23.

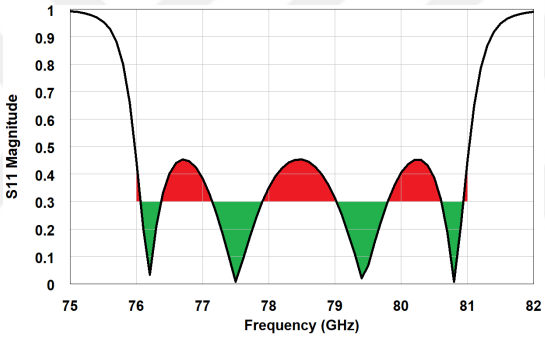


Figure 4.23: Summation of Penalties Representation

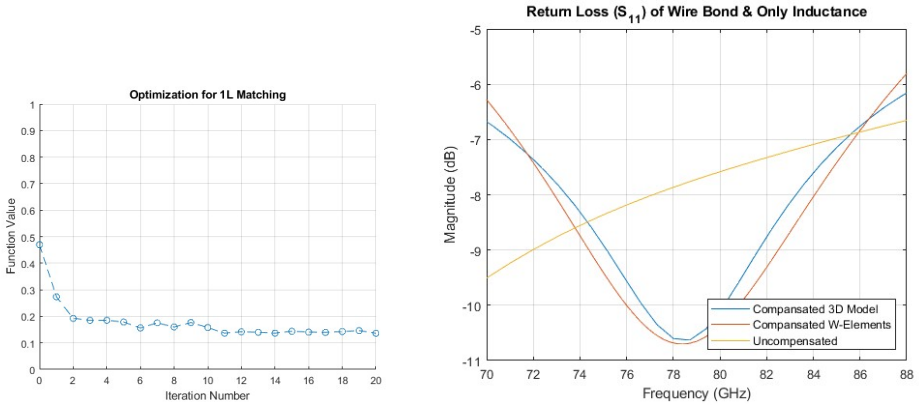
In this exemplary case, the target $|S_{11}|$ value is 0.3 (in linear) for the 76-81 GHz frequency band. The green parts satisfy this condition, and they do not have any contribution to the error function, whereas the error of the red parts is added to the function by their difference, as shown in Equation (4.6) substituting the $x_{11} = 10^{|S_{11,instant}|/10} - 10^{|S_{11,target}|/10}$ identity. The sgn function returns with +1 when the instant value of $|S_{11}|$ is higher (worse) than the target value and an error is added. However, sgn returns with -1 when $|S_{11}|$ is lower (better) than the target, and it cancels the multiplication term, and no error is added.

$$F_{error_{S11}} = \sum_{f=f_1}^{f_2} (x_{11})(\frac{1 + sgn(x_{11})}{2}) \tag{4.6}$$

In addition to the length change, the width of the matching section varied with the help of a similar procedure. As specified by the vendor, the minimum manufacturing width is three mils while the maximum width is dictated by the distance between the adjacent RX channels, which is 30 mils. This range is divided by one mil steps and 28 different RLGC models are obtained. Then, the optimization algorithm chooses a suitable width and length combination within the boundary. According to the number of errors, the width can be changed stepwise, and the length can be changed in a continuous spectrum. After the observation of necessary improvements in RL, the objective function of the optimization is updated to minimize the overall value. By doing so, a compromise point between $|S_{11}|$ and $|S_{21}|$ improvements can be found without assigning optimization weights manually. This objective function can be expanded to an error function given in Equation (4.7) by adding $x_{21} = 10^{|S_{21,instant}|/10} - 10^{|S_{21,target}|/10}$.

$$F_{error_{S11,S21}} = \sum_{f=f_1}^{f_2} \left(x_{11}(\frac{1+sgn(x_{11})}{2}) + x_{21}(\frac{1+sgn(x_{21})}{2}) \right) \tag{4.7}$$

When the effect of the inductive section is observed from Figure 4.24, it is seen that within the first three iterations, the function value lowers sharply, suggesting a quick initial convergence. This proves that the technique works well for rapidly locating a near-optimal area. The numbers peak at iterations 6-7, indicating that either the algorithm has stabilized or the answer is near the global minimum. A significant mismatch in the uncompensated design is represented by the initial function value of 0.5. The final function value stabilizes above 0.1, indicating a notable improvement and probably satisfying the necessary design requirements. The smoothness of the curve shows that the optimization process is stable and immune to local minima and numerical problems. In terms of the RL value, particularly close to 77 GHz, the compensated 3-D model and compensated W-elements both achieve reduced RL as compared to the uncompensated situation. It shows that the adjusted impedance matching was successful. Near the target frequency, these instances exhibit a low RL (-10 dB), but the uncompensated design stays over -8 dB. The tight alignment of the orange and blue curves indicates that the W-element approximation successfully reproduces the 3D model performance. Poor impedance matching and increased reflection across the band are shown by the comparatively flat response of uncompensated design.



(a) Objective Function Value

(b) Model Result Comparison

Figure 4.24: RL ($|S_{11}|$) Effect of Only Inductive Section

Afterwards, the matching process starts at one stage of the LC section. The necessary W-element model is constructed as in Figure 4.25. The discontinuity models between the combinations of through, capacitive, and inductive lines are already defined. The only dependent parameter is the capacitances parallel to the narrow line sections since the change of lengths affects this value according to the surface equation given previously.

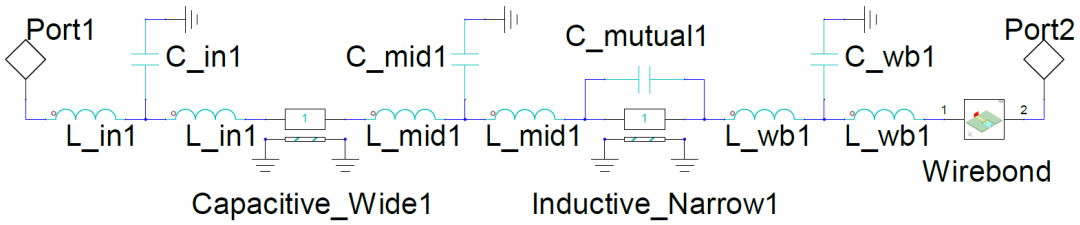
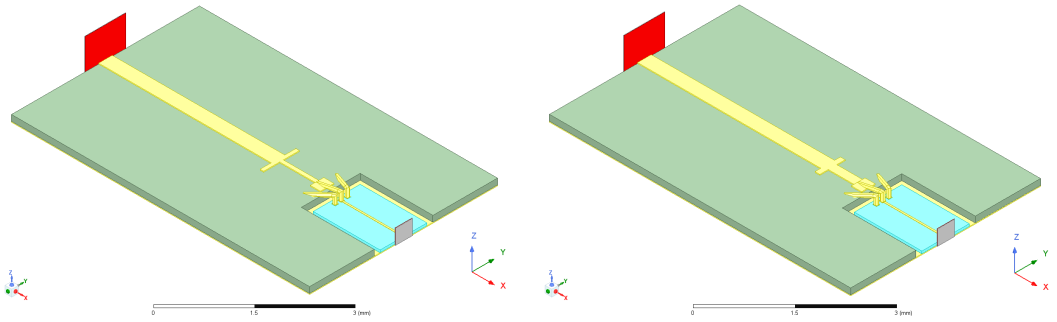


Figure 4.25: Complete W-Element Model for 1 Stage LC Matching

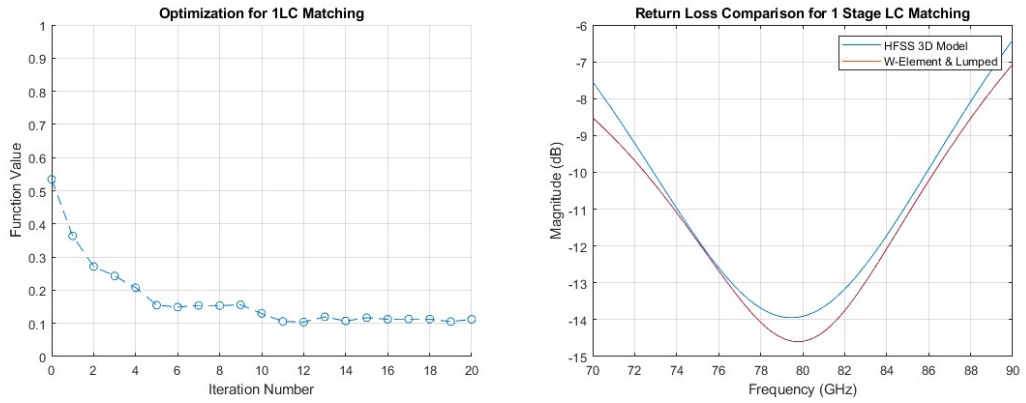
The isometric view of the HFSS models is shown in Figure 4.26. The primitive version of the optimization algorithm used a constant of 30 mils of wide and three mils of narrow line widths, and it only manipulated the lengths of these sections. However, better RL results can be achieved within a smaller area by assigning varying widths among the 3-30 mils range with one mil resolution. Hence, two different models are given for comparison regarding the degree of freedom on the width dimension.



(a) Constant Widths (b) Varying Widths

Figure 4.26: HFSS Model for 1 Stage LC Matching

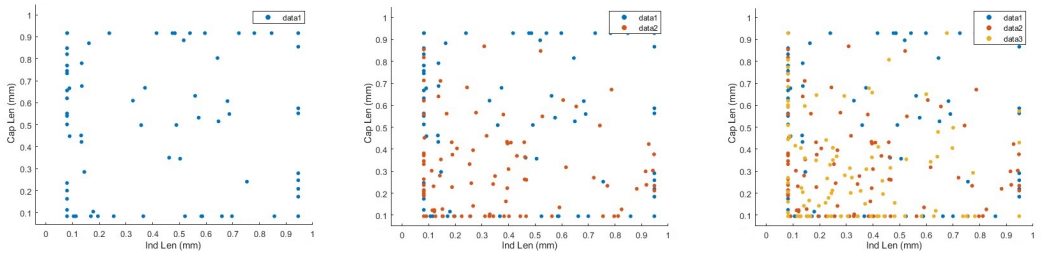
After the successive lumped element implementation into the W-element model, the RL result of the 1-LC case is predictable, as shown in Figure 4.27. If the objective function graph is examined numerically, the starting function value in the only L case was around 0.5. The initial function value in the 1-LC case is around 0.45, which is lower than the only L case. The function value of 0.12 is where the 1-L graph stabilizes, while the 1-LC graph seems to stabilize at a lower value (nearer to 0.1), indicating better optimization performance. The third iteration essentially completes the steep fall in the 1-L graph. The drop in the 1-LC graph takes a little longer, up to four or five iterations. The slower convergence of this new graph indicates a more precise or robust optimization that trades speed for the minimization of the objective function. Variations in the initial circumstances and algorithmic parameters, such as termination criteria or learning rate, might cause these discrepancies. In terms of the depth of RL, the 1-L design was at about -10 dB, while much better impedance matching was obtained by LC matching. The 1-LC matching exhibits better matching across a wider frequency range in addition to deeper RL. With respect to the complexity of design, the 1-LC matching network shows a more complicated optimization procedure for the application. This comparison emphasizes how crucial the combined usage of L and C components is to attaining better impedance matching at high frequencies.



(a) Objective Function Value (b) Model Result Comparison

Figure 4.27: RL ($|S_{11}|$) for 1 Stage LC Matched Bond

From this application perspective, the optimization algorithm (objective function value) shows some plateau regions. In these regions, the algorithm might stuck in a specific width value for one of the sections and length change could not result in a better solution. The behavior of the particles are illustrated in Figure 4.28. In these exemplary iterations, the horizontal axis is the length of the inductive section while vertical shows the capacitive one. Particles are randomly initialized between lower and upper limits. The general behavior of the swarm is converging to the optimal length combination. If the movement of each particle is investigated separately, it is seen that some of the particles are diverges from the optimum point while most of them are converging.



(a) (b) (c)

Figure 4.28: Swarm Behavior of Particles within Iterations

Then, the matching process is continued with two-stage LC sections. The necessary W-element model is constructed as in Figure 4.29. The HFSS model is given in Figure 4.30.

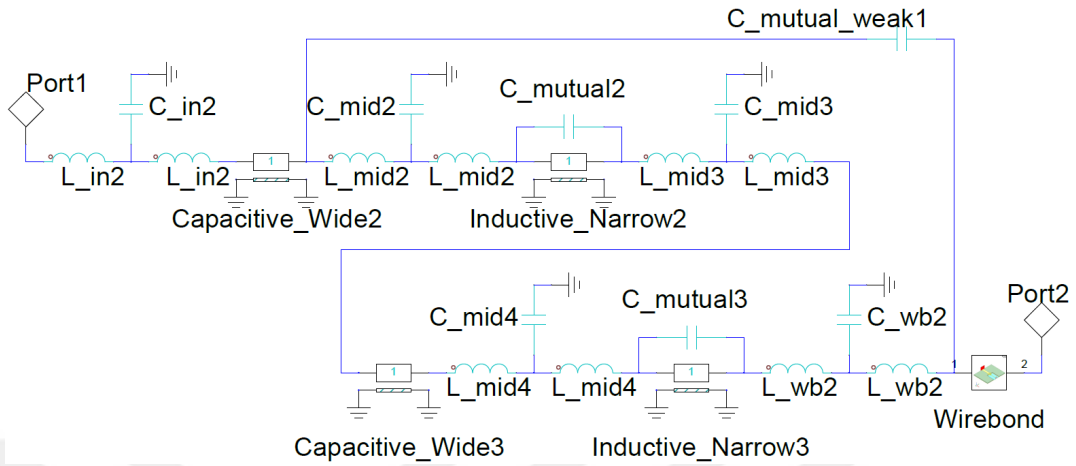
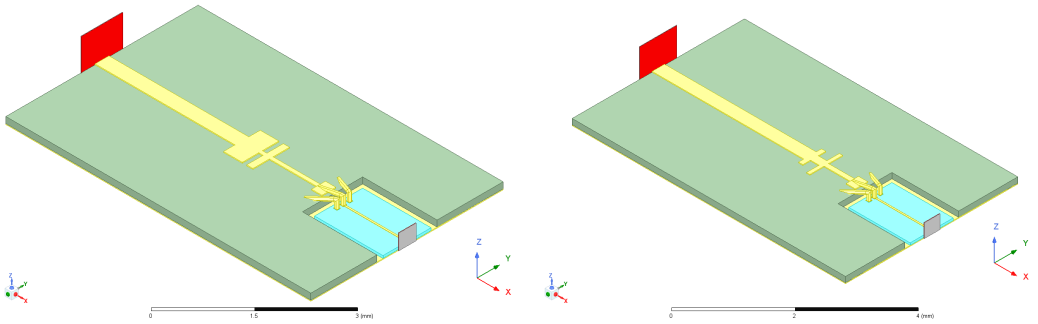


Figure 4.29: Complete W-Element Model for 2 Stage LC Matching



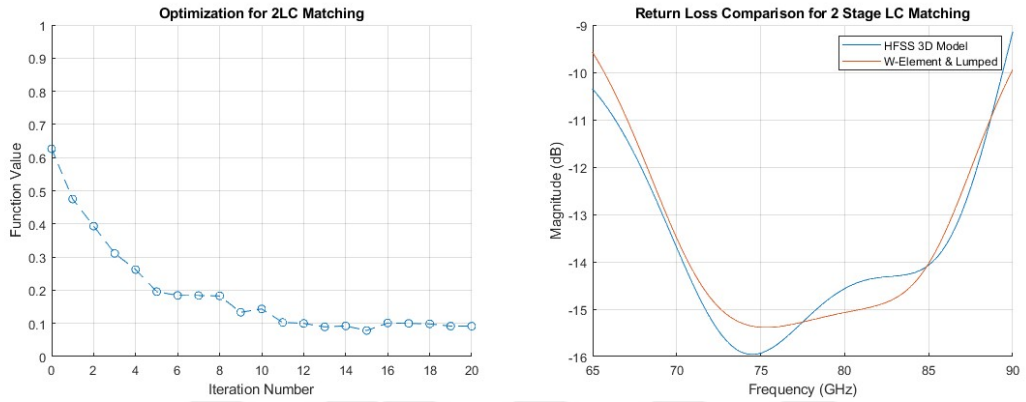
(a) Constant Widths

(b) Varying Widths

Figure 4.30: HFSS Model for 2 Stage LC Matching

Hence, results are compared with each other as seen in Figure 4.31. From the new objective function value graph, one can observe that the algorithms exhibit a similar trend. This suggests that the optimization quickly finds an initial good solution and then refines it further with subsequent iterations. It is seen that the 1-L and 1-LC cases appear to converge more quickly than the 2-LC comparing the three cases. The function value of the 1-L and 1-LC reaches a plateau after around ten iterations, while

the 2-LC continues to improve slightly beyond that point. This suggests that the 1-L and 1-LC algorithms may be more efficient in finding a good solution, but the 2-LC is capable of achieving a better final solution. From the RL point of view, compared to the one-stage LC-matched bond, the two-stage configuration exhibits a wider BW of low RL, indicating improved impedance matching over a broader frequency range.



(a) Objective Function Value

(b) Model Result Comparison

Figure 4.31: RL ($|S_{11}|$) for 2 Stage LC Matched Bond

Lastly, the matching process is finished with three-stage LC sections. The necessary W-element model is constructed as in Figure 4.32. The HFSS model is given in Figure 4.33.

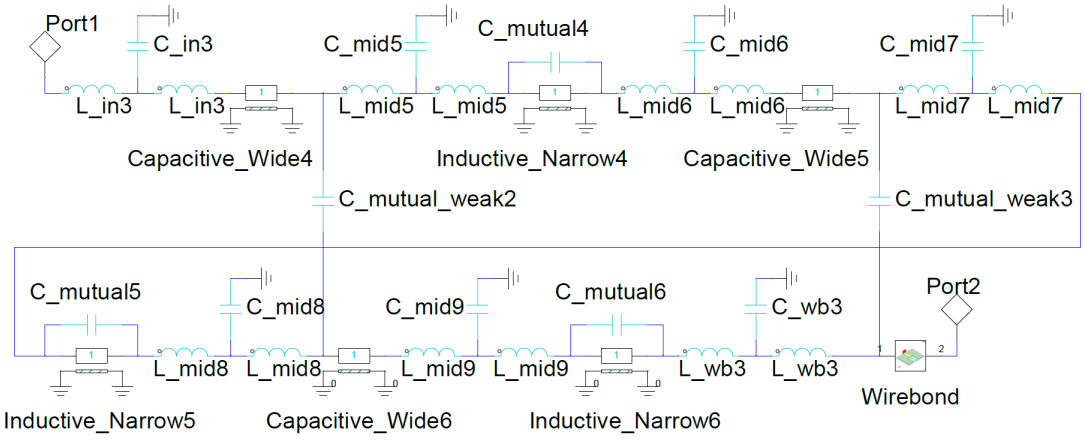
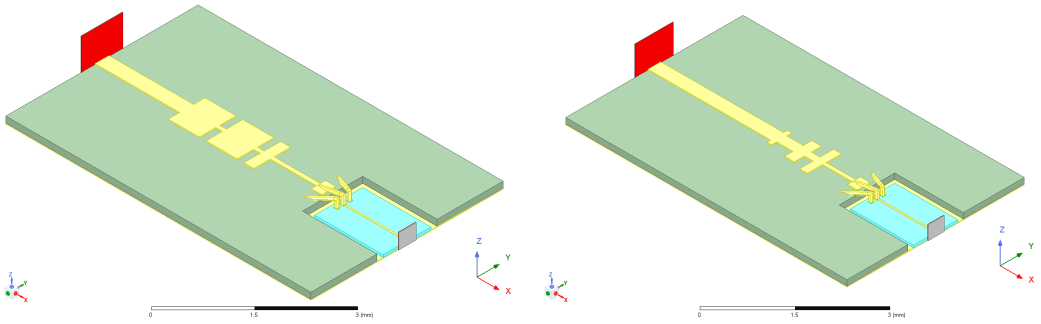


Figure 4.32: Complete W-Element Model for 3 Stage LC Matching

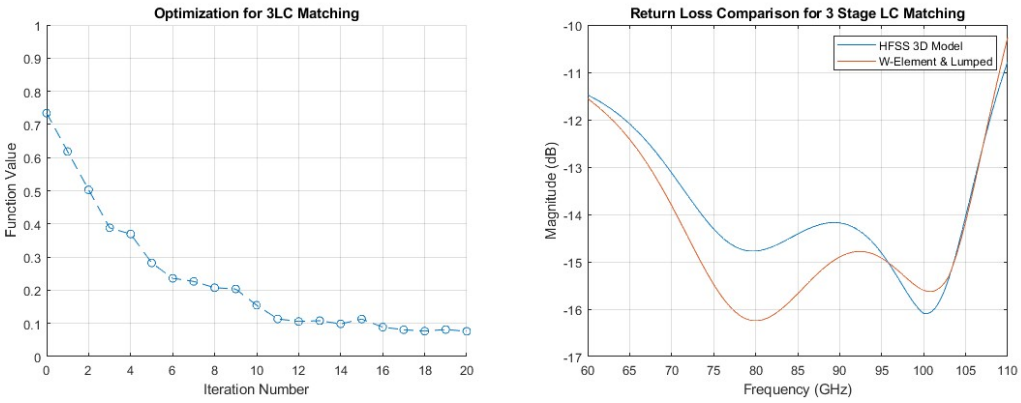


(a) Constant Widths (b) Varying Widths

Figure 4.33: HFSS Model for 3 Stage LC Matching

Hence, results are compared with each other as seen in Figure 4.34. Since the number of stages is increased up to 3 in this case, the expected matching BW is wider. This leads to the highest initial objective function value, which is above the 0.7 level. The rate of decay is lowered because the combination of width and length values covers a more significant sample space. There are relatively flat areas between the iterations where the algorithm might get stuck at a specific dimension, and the optimization cost barely declines. Overall, the function value decreased below 0.1 value at the 20^{th} iteration. If the RL characteristics are compared, the BW is improved in both HFSS and W-element models when the -10 dB is taken as a rule of thumb. In the middle of the matching BW, there is a 1 dB numerical difference between models where it corresponds to 8‰ reflected power error in the linear scale. Even so, this phenomenon indicates the W-element model can still be improved by adding other possible interactions.

In the last version of the MATLAB optimization code, the number of stages is defined as an optimization parameter. This change requires defining the objective function again because it was dependent on the sum of penalties. In the new version, the sum of penalties is replaced by the average of the sum of penalties. Previously obtained F_{error} is multiplied by the total frequency BW, which satisfies the target, and divided by the total BW as shown in Equation (4.8). To be specific, there are total of $(f_2 - f_1)/\Delta f$ frequency intervals from f_1 to f_2 with Δf steps. For example, there are 150 intervals between 71-86 GHz with 0.1 GHz steps. If the target is satisfied only in 76-81 GHz



(a) Objective Function Value

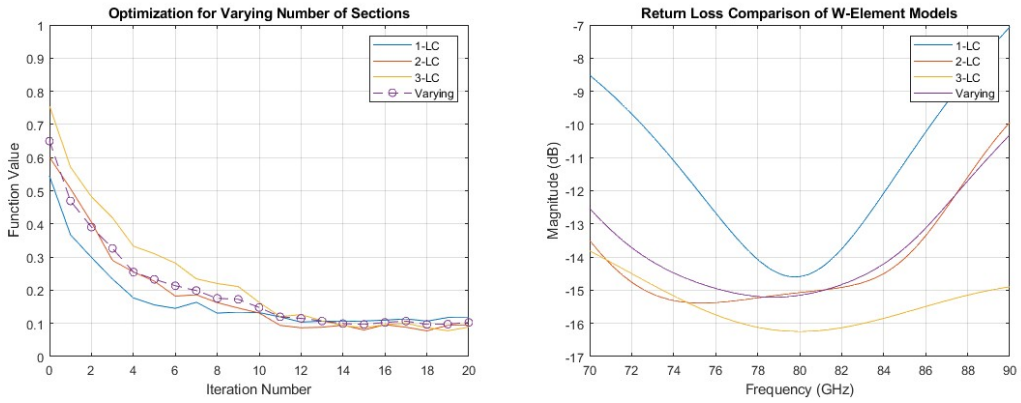
(b) Model Result Comparison

Figure 4.34: RL ($|S_{11}|$) for 3 Stage LC Matched Bond

intervals, then the summation of sgn values results in 50. Hence, the previous error function is multiplied with a 50/150 ratio to make a fair comparison between matched RL values of different numbers of stages.

$$F_{error_{AVG}} = \frac{F_{error_{S11,S21}}}{(f_2 - f_1)/\Delta f} \sum_{f_1+n\cdot\Delta f}^{f_2} \left(\frac{1 + sgn(x_{11})}{2} + \frac{1 + sgn(x_{21})}{2} \right) \tag{4.8}$$

Instead of making separate simulations and comparisons, this code automatically chooses the optimum number of sections. When more than one solution have a necessarily low residual error, then the algorithm selects the lower number of stages to make it easier for manufacturing and less dependent on tolerances. By this method, it is concluded that the 2-stage compensation model has the optimum RL and IL values with respect to its BW. The results of the new algorithm are not directly the same as the previous cases, as depicted in Figure 4.35. Due to the random nature of PSO and variances in initialization, deviations can occur even though the new fitness function and simulation technique are compatible with the previous implementation. The optimizer looks at combinations that were not taken into account in the individual tests since the search area is more extensive and allows for different stage numbers. By directing the optimizer toward regions of the search space that provide lower error values, the error function may prefer an alternative configuration. The algorithm can find solutions with fewer stages if they offer higher fitness scores by letting the stage number change as an optimization parameter. This frequently occurs as a result of variations in initialization or limitations and a more comprehensive exploration.



(a) Objective Function Value Comparison

(b) RL ($|S_{11}|$) Comparison

Figure 4.35: Performance Metrics for Varying Number of Stages

The figure of merit of the previous discussion was the optimization of the matching network postulating the necessity of this circuit. However, this structure always has added input IL value with respect to the 50 Ω through line having the same length of matching. Also, another option would be not using input and output lines at all and only using wire-bond interconnection. Table 4.2 shows the IL comparison between mainly three different cases. The "Wirebond" column shows the results of the direct interconnection of the input port to the previous antenna stage and the connection of the output port to the following transceiver stage. The "Equi-length TL" column indicates the result of the case where a through line whose length is equal to the length of the matching section. There is an increase of equivalent through-line losses, which is predicted due to the nature of loss on a longer path. In addition to that, the IL increases with the increasing number of matching sections within the same length. Also, there are multiple reflections at the discontinuity boundaries, which results in more lost power in signal transmission.

Table 4.2: Comparison of ILs for Matching Sections

Model Type	Wirebond	Equilength Line	Matching Lines
1 Stage	-1.07 dB	-1.10 dB	-1.19 dB
2 Stage	-1.07 dB	-1.22 dB	-1.46 dB
3 Stage	-1.07 dB	-1.54 dB	-1.93 dB

The difference of objective function values between these three different cases are summarized in Table 4.3 in terms of both linear and decibel scales. The improvement is maximized in 2 stage matching when these values are compared. The linear difference can be seen as low but the effect is more apparent in the dB scale.

Table 4.3: Objective Function Values for Different Cases

Model Type	Linear Scale	Decibel Scale
1 Stage	0.1097	-19.96 dB
2 Stage	0.0924	-20.69 dB
3 Stage	0.1015	-19.87 dB

It is seen that adding through lines or matching circuits increases the IL, and the NF value is negatively affected. However, there is already 1 cm gap between the RX pad of transceiver and RX antennas in this specific application. This gap is inserted intentionally to create better isolation between the TX and RX antennas of the transceiver. A signal with a magnitude of ($P_{out_{TX}} - P_{coupling}$) leaks to the RX side, and this signal is amplified by the LNA. This pre-amplified leakage signal level could be high, and it could saturate the RX components, which is not desired for identification. Hence, this 1 cm gap can be used for both LNA and input-output matching circuits. The only practical loss is the difference between the equal length through line and compensation network since the direct connection is not applicable.

CHAPTER 5

CONCLUSIONS

In conclusion, this research offers a thorough exploration of optimizing die-on PCB design for E-band LNAs, focusing on factors critical to high-frequency RF applications such as NF and S parameters. The methodology of the study, which includes a literature review, analytical derivations, and extensive simulations followed by experimental validation, demonstrates the impact of various design parameters on LNA performance. By examining the effects of line types, including microstrip and CPWG, via distribution and wire bond dimension parameters (width, length, height, and number of bonds), an optimum uncompensated model is achieved. After the manufacturing, S-parameters of different through-line PCBs are measured, and the IL effect of the PCB finishing is confirmed. The manufactured uncompensated LNA design is also measured by using the transceiver IC as a signal generator, and the 21 dB gain, 17 dBm saturated output power, and 6 dB NF specifications are approved for this case. The main of the thesis was the design and optimization of compensation configurations. The proposed hybrid model includes W-element models for matching sections and lumped element equivalents of mutual capacitances and asymmetric discontinuity models. This new circuit model is adapted to MATLAB, and the width, length, and number of the capacitive and inductive sections are optimized using PSO. 1-2-3 stage compensation networks are firstly optimized in length by keeping widths constant. Then, these widths are also assigned as variables. Finally, the number of stages is implemented as another optimization variable. The defined objective function is based upon the instant and targeted value, which measures the remaining signal level after the subtraction of RL and IL values. This research identifies key strategies for enhancing gain, reducing RL, and keeping NF at a minimum. The findings, specifically regarding the Analog Devices HMC8325 die, provide valuable insights and practi-

cal solutions for improving LNA design in both civilian and military applications, thereby contributing significantly to the field of RF microwave engineering.

The correctness of the results and compilation time of various optimization techniques will be carefully examined in further research, with an emphasis on low and multi-fidelity techniques. The Particle Swarm Optimization (PSO) technique will calculate the objective function value in the low-fidelity approach using the hybrid (W-element) model findings. The top ten cases, along with ten randomly chosen cases, will undergo full-wave simulations in HFSS when this value is minimized. After that, the PSO will include these simulation findings once more for additional improvement. In contrast, HFSS simulations will be used directly throughout the optimization phase in the multi-fidelity method. It will be determined that the hybrid model provides a more workable option for applications with stringent time limitations if it shows a significant decrease in calculation time with acceptable accuracy when compared to HFSS. The broader problems of optimization in EM system design can be addressed by further research avenues outside this comparison. Subsequent research endeavors may concentrate on improving hybrid models to encompass a greater variety of materials and geometries. In order to anticipate model errors and dynamically correct them, this endeavor can entail using machine learning techniques. Alternative optimization approaches like genetic algorithms (GA), or Bayesian optimization might be investigated to assess their effectiveness compared to PSO in terms of convergence rate and computing efficiency. The design process may be sped up even further by combining these techniques with manufactured models. Incorporating measured data from manufactured prototypes into the optimization framework helps guarantee that the models are both computationally efficient and highly realistic of real-world situations. The scalability of these optimization methods should be examined in light of the continued interest in higher GHz and THz ranges. Examining the effects of parasitic and nonlinearity, which become more noticeable at higher frequencies, is part of this. The feasibility of these techniques for industrial applications may be improved by creating completely automated processes that smoothly connect hybrid models, full-wave simulations, and production limitations.

REFERENCES

[1] G. R. Reddy, "Advancements in high-frequency vlsi designs for 5g and future telecommunications technologies," *International Journal of Research Publication and Reviews*, vol. 5, pp. 1833–1840, February 2024.

[2] V. Petrov, M. Komarov, D. Moltchanov, J. M. Jornet, and Y. Koucheryavy, "Interference analysis of ehf/thf communications systems with blocking and directional antennas," in *2016 IEEE Global Communications Conference (GLOBECOM)*, pp. 1–7, 2016.

[3] K. Ramasubramanian, K. Ramaiah, and A. Aginskiy, "Moving from legacy 24 ghz to state-of-the-art 77 ghz radar," Tech. Rep. SPRY312, Texas Instruments, Dallas, Texas, October 2017.

[4] D. M. Pozar, *Microwave engineering: theory and techniques*. John wiley & sons, 2021.

[5] U. Pfeiffer, J. Grzyb, D. Liu, B. Gaucher, T. Beukema, B. Floyd, and S. Reynolds, "A chip-scale packaging technology for 60-ghz wireless chipsets," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 8, pp. 3387–3397, 2006.

[6] M. Schober, A. Chico, D. del Rio, and V. Ermolov, "Embedded component packaging for d-band radio systems," 06 2024.

[7] ANSYS Inc., "Ansys hfss." `https://www.https://www.ansys.com`, 2024. Release 2024R1.

[8] Texas Instruments, *AWR2243 Single-Chip 76- to 81-GHz FMCW Transceiver*, February 2024. Rev. D.

[9] Analog Devices, *HMC8325: 71 GHz to 86 GHz E-Band Low Noise Amplifier*, February 2017. Rev. 0.

[10] Y. Zhang, M. Sun, K. Chua, L. Wai, and D. Liu, "Antenna-in-package design for wirebond interconnection to highly integrated 60-ghz radios," *Antennas and Propagation, IEEE Transactions on*, vol. 57, pp. 2842 – 2852, 11 2009.

[11] W. Tian, H. Cui, and W. Yu, "Analysis and experimental test of electrical characteristics on bonding wire," *Electronics*, vol. 8, no. 3, p. 365, 2019.

[12] F. Alimenti, P. Mezzanotte, L. Roselli, and R. Sorrentino, "Modeling and characterization of the bonding-wire interconnection," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 1, pp. 142–150, 2001.

[13] C.-C. Wei, C.-T. Fan, T.-H. Chiang, M.-K. Chiu, and S.-P. Ru, "A comparison study of high-frequency performance between ball bonding and ribbon bonding," in *2009 4th International Microsystems, Packaging, Assembly and Circuits Technology Conference*, pp. 685–688, 2009.

[14] S. T. Choi, K. S. Yang, K. Tokuda, and Y. H. Kim, "60-ghz transceiver module with coplanar ribbon bonded planar millimeter wave bandpass filter," *Microwave and Optical Technology Letters*, vol. 49, no. 5, pp. 1212–1214, 2007.

[15] K. Samanta, D. Stephens, and I. Robertson, "Design and performance of a 60 ghz multi-chip-module receiver employing substrate integrated waveguides," *Microwaves, Antennas and Propagation, IET*, vol. 1, pp. 961 – 967, 11 2007.

[16] G. Liu, A. Trasser, A. Çağri Ulusoy, and H. Schumacher, "Low-loss, low-cost, ic-to-board bondwire interconnects for millimeter-wave applications," in *2011 IEEE MTT-S International Microwave Symposium*, pp. 1–4, 2011.

[17] B. J. Lameres and S. P. Khatri, "Broadband impedance matching for inductive interconnect in vlsi packages," *2005 International Conference on Computer Design*, pp. 683–688, 2005.

[18] Z. Wang, J. Gao, G. Flowers, K. Song, W. Yi, and Z. Cheng, "Investigation of impedance compensation in radio frequency circuits with bonding wire," *International Journal of RF and Microwave Computer-Aided Engineering*, vol. 32, 03 2022.

[19] M. Lippoldt, "Bond-wire impedance compensation for millimeter-wave chip interconnects," 2020.

[20] V. Valenta, T. Spreng, S. Yuan, W. Winkler, V. Ziegler, D. Dancila, A. Rydberg, and H. Schumacher, "Design and experimental evaluation of compensated bondwire interconnects above 100 ghz," *International Journal of Microwave and Wireless Technologies*, vol. 7, pp. 1–10, 03 2015.

[21] M. Umar, M. Laabs, N. Neumann, and D. Plettemeier, "Bondwire model and compensation network for 60 ghz chip-to-pcb interconnects," *IEEE Antennas and Wireless Propagation Letters*, vol. 20, no. 11, pp. 2196–2200, 2021.

[22] W. Jiang, M. Tang, J. Mao, H. Yue, and Y. Tang, "A novel compensation technique for bonding-wire interconnection based on single-objective optimization in millimeter-wave band," in *2018 International Conference on Microwave and Millimeter Wave Technology (ICMMT)*, pp. 1–3, 2018.

[23] F. Harris and C. Dick, "Snr estimation techniques for low snr signals," pp. 276–280, 01 2012.

[24] M. Capek, L. Jelinek, and P. Hazdra, "On the functional relation between quality factor and fractional bandwidth," *IEEE Transactions on Antennas and Propagation*, vol. 63, no. 6, pp. 2787–2790, 2015.

[25] R. Ludwig and P. Bretchko, *RF Circuit Design: Theory and Applications*. Pearson Education, 2000.

[26] C. Bowick, J. Blyler, and C. Ajluni, *RF Circuit Design*. Electronics & Electrical, Elsevier/Newnes, 2008.

[27] R. Pierret, *Semiconductor Device Fundamentals*. Addison-Wesley, 1996.

[28] T. Kawasaki, A. Otsuka, M. Kubota, T. Tokumitsu, and Y. Hasegawa, "Millimeter-wave low noise amplifiers suitable for flip-chip assembly," Tech. Rep. Number 81, Sumitomo Electric Industries, Kanagawa, Japan, October 2015.

[29] Macom, *CG2H40045: 45 W, DC - 4 GHz RF Power GaN HEMT*, August 2022. Rev. 3.1.

[30] "Rf material overview for mmwave radar applications," Tech. Rep. Publication 92-130, Rogers Corporation, Chandler, AZ, January 2018.

[31] A. Djordjevic, M. Stojilović, and T. Sarkar, "Closed-form formulas for frequency-dependent per-unit-length inductance and resistance of microstrip transmission lines that provide causal response," *IEEE Transactions on Electromagnetic Compatibility*, vol. 56, pp. 1604–1612, 12 2014.

[32] "Ro3000 series circuit materials," Tech. Rep. Publication 92-130, Rogers Corporation, Chandler, AZ, 2024.

[33] "Astra mt77 ultra low loss, rf/mw laminate and prepreg," Tech. Rep. E41625, Isola Group, RoadChandler, AZ, March 2024.

[34] S. Hinaga, A. Rakov, M. Koledintseva, and J. Drewniak, "Insertion loss reduction through non-roughening inner-layer surface treatments," *IPC APEX EXPO 2014*, January 2014.

[35] "High frequency electronics product selector guide," Tech. Rep. Publication 92-601, Rogers Corporation, Chandler, AZ, December 2023.

[36] A. Atiqah, A. Jalar, M. Abu Bakar, and N. Ismail, *Advancement of Printed Circuit Board (PCB) Surface Finishes in Controlling the Intermetallic Compound (IMC) Growth in Solder Joints*, pp. 217–238. 03 2022.

[37] M. George, "Minimizing signal transmission loss in high-frequency circuits," Tech. Rep. IConnect-007, Uyemura Advanced Plating Chemistries, Ontario, California, July 2020.

[38] D. J. Rasmussen, "Gold ball wire bonding with heated tool for automotive microelectronics," Tech. Rep. Section 3.1.5.3, Palomar Technologies, Carlsbad, CA, July 2017.

[39] M. Seyyedesfahlan, *On-chip antennas and PCB packaged phased-array radar receiver front-end at mm-wave frequencies*. PhD thesis, Sabanci University, 2015.

[40] W.-C. Wu, L.-H. Hsu, E. Y. Chang, C. Karnfelt, H. Zirath, J. P. Starski, and Y.-C. Wu, "60 ghz broadband ms-to-cpw hot-via flip chip interconnects," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 11, pp. 784–786, 2007.

[41] Sumitomo Electric Industries, *SMM5727XZ: 71–86 GHz Low Noise Amplifier MMIC*, December 2014. Edition 1.0.

[42] "Thz chip list by chip function," Tech. Rep. Version: 202406141, MKR Tech, Chengdu, China, June 2024.

[43] M. Kozlov and R. Turner, "A comparison of ansoft hfss and cst microwave studio simulation software for multi-channel coil design and sar estimation at 7 t mri," *Piers Online*, vol. 6, pp. 395–399, 01 2010.

[44] IEEE EPS Technical Committee on Electrical Design, Modeling and Simulation, "Packaging Benchmark Suite," 2021. [Online; accessed 2022-03-16].

[45] C. Kumar, A. Kumar, , and R. Rosales, "mmwave radar sensor rf pcb design, manufacturing and validation guide," Tech. Rep. SPRACG5, Texas Instruments, Dallas, Texas, May 2018.

[46] A. Youmsi, "01k80a-40ml5: Smd connector jack rpc-1.00," Tech. Rep. h00, Rosenberger GmbH, Tittmoning, Germany, March 2022.

[47] J. Lim, D. Kwon, J.-S. Rieh, S.-W. Kim, and S. Hwang, "Rf characterization and modeling of various wire bond transitions," *IEEE Transactions on Advanced Packaging*, vol. 28, no. 4, pp. 772–778, 2005.

[48] M. Arifin, N. Wivanius, and N. F. Prebianto, "Epoxy adhesive as die attach material in semiconductor packaging: A review," in *2018 International Conference on Applied Engineering (ICAE)*, pp. 1–5, 2018.

[49] M. Zarei, A. Khalilzadegan, and K. Hadidi, "Design analysis and evaluation of a w-element model for a twisted-pair cable," *IEEE Access*, vol. 8, pp. 188981–188992, 01 2020.

[50] Y. Awasthi, H. Singh, and A. Verma, "Computer-aided design modeling of microstrip step discontinuity on multilayer iso/anisotropic substrates with transient signal analysis," *Springer Nature Applied Sciences*, June 2019.

[51] C. H. Wu, G. Zhou, P. Ma, Y. Wu, K. Li, L. Shen, Q. Shen, H. Zhang, J. Yan, Y. You, J. Shen, X. Wang, C.-C. Chang, and F. He, "Analysis of the electromagnetic interaction between periodically corrugated transmission lines through the

mutual capacitance and mutual inductance," *IEEE Access*, vol. 10, pp. 15818–15834, 2022.

[52] K. Gupta, R. Garg, and R. Chadha, *Computer-aided Design of Microwave Circuits*. Artech Microwave Library, Artech, 1981.

[53] E. İşcan, "Design of a tunable wideband bandpass filter based on substrate integrated waveguide technology for channelized receivers," Master's thesis, Middle East Technical University, 2024.

APPENDIX A

PSO ALGORITHM KEY CONCEPTS

The social behavior of creatures, such as fish schools or flocks of birds, serves as the inspiration for PSO. All particles share a global best value that represents the best solution found by the swarm, and each particle keeps its own personal best position, which means the most ideal solution it has come across. According to its velocity adjustment, each particle tries to move toward its personal best position. Acting as a benchmark for updates, the global best guides the particles towards the optimal solution discovered. The particles adjust their positions in accordance with the computed velocities, and this process keeps going until a predetermined stopping criterion, like hitting a preset objective value or reaching the maximum number of iterations, is satisfied. This termination criteria indicates when the algorithm should cease. Examples of typical stopping conditions include reaching a maximum number of iterations, converging to a designated error threshold, or when the global best solution shows no substantial improvement. The simplicity of PSO, which requires fewer parameters than alternatives like genetic algorithms, and its adaptability, which allows it to be used for a variety of issues ranging from continuous to discrete optimization, set it apart from other optimization techniques. Furthermore, it is especially appealing for engineering applications due to its rapid convergence and resilience in a variety of situations. PSO can, however, encounter difficulties, such as early convergence to local optima in intricate environments, which are frequently alleviated by adjusting parameters or combining them with other methods. Because of its simplicity of use, PSO continues to be a valuable tool in optimization research and real-world applications.