A READOUT CIRCUIT FOR RESONANT MEMS TEMPERATURE SENSORS

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ABSTRACT

A READOUT CIRCUIT FOR RESONANT MEMS TEMPERATURE SENSORS

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High precision is the dominant advantage that resonant sensors have over other types of analog sensors (sensors with a subsequent analog-to-digital converter). The resolution of these precise sensors is determined by both frequency resolution and sensitivity of the sensor. The sensitivity is highly related to the sensitivity of the MEMS resonator. However, the frequency resolution is dominantly defined by the closed-loop circuitry if noise contribution of the resonator is assumed to be smaller than that of the electronic circuitry. In this thesis, resolution reduction of a closed-loop resonant sensor is intended to be accomplished. The DETF (double-ended tuning-fork) MEMS resonator used in this study is already designed and fabricated in METU MEMS. The TCF (temperature coefficient of frequency) of this resonator is 53 ppm/K which results in a sensitivity of 9.27 Hz/K with 174.818 kHz resonant frequency. This implies that the sensitivity is fixed and the only remaining parameter to achieve a better resolution for the sensor is the frequency resolution of the closed-loop circuitry.

Since closed-loop with an AGC (automatic gain control) block has superior far-from-carrier phase noise performance in comparison to a closed-loop circuit with a limiter

(e.g., comparator), this scheme is chosen to be implemented in XFAB 0.35μm CMOS process. For the implemented closed-loop circuit in CMOS technology, the minimum achievable noise floor at the steady state oscillation is obtained to be -107 dBc/Hz. Based on the simulation results, when the "white phase" noise is filtered out, the sensor resolution is obtained to be around 0.021 °C. To verify the functionality of the design in the CMOS technology, the closed-loop circuit is implemented again by discrete components. The stability and resolution evaluations of the implemented circuit are achieved by Allan deviation. The bias instability point is measured to be about 0.0045 °C with 5.28 second averaging time. In this thesis, the main goal of the design, especially in XFAB 0.35μm CMOS Process, is to study and characterize the noise and phase noise performances of the closed loop circuit. Thus, the resolution improvement can be accomplished by minimizing the noise in the loop.

Keywords: Resonant Sensor, DETF MEMS Resonator, Closed-loop Circuit, Frequency Stability, Phase Noise, Allan Deviation, CMOS Based Circuit Design.

ÖZ

REZONANS MEMS SICAKLIK SENSÖRLERİ İÇİN OKUMA DEVRESİ

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Rezonans sensörlerin yüksek hassasiyeti, analog-digital dönüştürücüye sahip olan diğer analog sensör tiplerine göre en önemli avantajıdır. Bu hassas sensörlerin çözünürlüğü, frekans çözünürlüğü ve sensörün hassasiyeti ile tespit edilmektedir. Hassasiyet, MEMS resonatörünün hassasiyetiyle yüksek ölçüde bağlantılıdır. Bununla birlikte eğer rezonatörün gürültü katkısı elektronik devresininkinden küçük olduğu farz edilirse frekans çözünürlüğü kapalı döngü devresi tarafından tanımlanabilir. Bu tez çalışmasında, kapalı döngü rezonans sensörün çözünürlüğünü, frekans çözünürlüğünü düşürerek geliştirilmesi hedefi başarılmıştır. Sıcaklık sensörü olarak kullanılan DETF (Çift Uçlu Diyapazon) MEMS rezonatör ODTÜ MEMS merkezinde önceden tasarlanmış ve üretilmiştir. DETF MEMS rezonatörün TCF'si (Frekansın sıcaklık katsayısı) 53 ppm/K'dir, ki bu duyarlılığın 174.818 kHz frekansında 9.27 Hz/K olmasını sağlamaktadır. Bu belirtiyor ki hassasiyet sabittir ve sensörün daha iyi bir çözünürlüğe ulaşması için geriye kalan tek değişken, kapalı döngü devresinin frekans çözünürlüğüdür.

AGC (Otomatik Kazanç Kontrol) bloğuna sahip kapalı döngü devresi, taşıyıcıdan uzak faz gürültü performansı limitleyiciye sahip kapalı döngü devresine kıyasla daha üstün performansa sahip olmasından mütevellit, bu topoloji XFAB 0.35m CMOS sürecinde yapılmak için seçilmiştir. CMOS Teknoloji'de yapılmış olan kapalı döngü devresi için kalıcı durum salınımında ulaşılabilecek en düşük gürültü dibi -107 dBc/Hz olarak belirlenmiştir. Simulasyon sonuçlarına göre "beyaz faz" gürültüsü filtrelendiğinde sensör çözünürlüğü yaklaşık olarak 0.021°C olarak belirlenmiştir. Dizaynın CMOS Teknoloji'sindeki işlevselliğini tahkik etmek için kapalı döngü devresi ayrık elemanlarla tekrar yapılmıştır. Uygulanan devrenin kararlılık ve çözünürlük değerlendirmesine Allan sapması ile ulaşılmıştır. Öngerilme kararsızlık noktası 5.28 saniye ortalama zamanda yaklaşık 0.0045°C olarak ölçülmüştür. Bu tezde, dizaynın özellikle XFAB'daki CMOS sürecindeki asıl amacı kapalı döngü devresinin gürültü ve faz gürültüsü performansını araştırmak ve nitelemektir. Bundan dolayı çözünürlük gelişmesi devredeki gürültünün düşürülmesiyle başarıya ulaşabilir.

Anahtar Kelimeler: Rezonans Sensörü, DETF MEMS Rezonatörü, Kapalı Döngü Devresi, Frekans Kararlılığı, Faz Gürültüsü, Allan Sapması, CMOS Temelli Devre Tasarımı.

To My Family
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LIST OF ABBREVIATIONS

DETF	Double-ended Tuning Fork
MEMS	Micro-electromechanical Systems
$L(f)$	Single Sideband Phase Noise
$S_\phi(f)$	Double Sideband Phase Noise
$S_y(f)$	Frequency Noise of the Closed-loop Circuit
σ_y^2	Allan Variance
f_{res}	Resonant Frequency of the MEMS Resonator
f_{osc}	Oscillation Frequency of the Closed-loop Circuit
η	Coupling Factor
CTV	Continuous-time Voltage Sensing
CTC	Continuous-time Current Sensing
τ	Relaxation Time of the Resonator
$\psi(t)$	Phase Fluctuation of the Open-loop Circuitry
$\phi(t)$	Phase Fluctuation of the Closed-loop Circuit
f_L	Leeson Frequency
γ	Noise Penalty
TIA	Trans-impedance Amplifier
VGA	Variable Gain Amplifier
GBW	Unity-gain Bandwidth
NBW	Noise Bandwidth
V_{PM}	Proof Mass Voltage
R_m	Motional Resistance of the Resonator
L_m	Motional Inductance of the Resonator
C_m	Motional Capacitance of the Resonator
R_f	Feedback Resistor of the Trans-impedance Amplifier
C_f	Feedback Capacitor of the Trans-impedance Amplifier
C_{ft}	Feed-through Capacitor
C_P or C_i	Input Parasitic Capacitance

CHAPTER 1

INTRODUCTION

1.1 Introduction and Motivation

The output of a resonant sensor is frequency modulated by the quantity being measured. The modulated signal can be measured, demodulated and digitized by other electronic stages to produce a signal proportional to the quantity to be measured. A significant advantage of resonant sensors with an intrinsic frequency output over other types of analog sensors with a subsequent analog-to-digital conversion stages is their frequency shift output signal. Frequency shift nature of the output signal provides a straightforward connection to a modern digital signal processing instrument. It means a safe transmission from the sensor element to electronics is possible. Output signal of a resonant sensor can be precisely measured and converted to digital form by counting zero crossings. This way of measurement inherently provides a higher precision [1, 2].

Resolution of these precise sensors (minimum detectable quantity change), as shown by Wojciechowski in [3], is proportional to the frequency resolution of the sensor (minimum detectable frequency change) and has an inverse proportionality to the sensitivity of the sensor as will be shown in section 2.5.2.4. If the noise contribution of the resonator is considered to be smaller than the noise contribution of the electronic circuitry, it can be concluded that the frequency resolution is determined by the electronic circuitry and resonator has the minimum role. On the other hand, sensitivity of the sensor is determined dominantly by the MEMS (Micro-electromechanical Systems) resonator. For instance, in the case of temperature sensor, which is the case

study in this thesis, sensitivity of the MEMS resonantor to temperature is about 53 ppm [4] while sensitivity of the electronic circuitry, as will be shown later in chapter three, is less than 100 ppb.

As a result, in order to get a better sensor resolution, frequency resolution of the closed-loop electronic circuit can be improved as the first step. Frequency resolution is improved by reducing Phase noise (or equivalently reducing frequency noise or Allan deviation). Second way to increase the sensor resolution is to increase the sensitivity of the sensor which is mostly determined by the MEMS resonantor sensitivity. A comparison is done in [5] among Resonant, Piezoelectric and Capacitive sensing techniques. It has been shown that the resolution of a resonant sensor is in 1 part in 10^8 while capacitive and peizoelectric sensing provide resolution in the range of 1-10 part in 10^5. That's why when the driving factor is precision, resonant sensors are used.

The DETF (Double-ended Tuning Fork) MEMS resonantor which is employed in the closed-loop circuit in this thesis has been designed and fabricated by Mr. Talha Köse in METU MEMS [4]. It implies that there is no control on the sensitivity of the sensor and the only remaining factor to improve sensor resolution is the frequency resolution of the closed-loop electronic circuitry. Frequency resolution reduction is done in this thesis with two main assumptions. Fisrt, noise contribution of MEMS resonator to the output noise of the closed-loop circuit is small in comparison to electronic circuitry's noise contribution. Second, MEMS resonator operates at its linear regime at steady state. First assumption is made because of the fact that in the simulations noise contribution of the MEMS resonator is ignored, it might be a valid assumption for high quality factor resonators. If in any case noise contribution of the resonator is comparable to that of electronic circuitry, phase noise can be simply analyzed in a way that is represented in [6]. Second assumption is made because in [7–10] it has been shown that the nonlinear behavior of resonator may provoke new PSD (Power Spectral Density) components at close-to-carrier phase noise. This occurs due to A-f effect (section 2.1.7) which results in some sort of amplitude-to-frequency conversion.

After defining the goal of the design which is "sensor resolution improvement by re-

ducing far-from-carrier phase noise", the resolution evaluation method becomes the next parameter that needs to be considered in the design. Generally closed-loop circuits take advantage of some sort of amplitude limiting technique (e.g., automatic gain control, limiter and comparator), because of this fact, fluctuations in the amplitude become less important for us and dominantly we try to assess fluctuations in the phase (or equivalently in the frequency). Fluctuations in amplitude might become important for us when some sort of amplitude to phase modulation happens in the loop.

Frequency stability analyses have been developed in the literature to evaluate the performance of a closed-loop circuitry. Phase noise and frequency noise (resolution per Hz) evaluate the noise performance of the closed-loop circuits in frequency domain [3, 6, 11–15] and Allan deviation evaluates noise performance in time domain [16, 17]. Sinusoidal wave closed-loop circuit with an automatic gain control block (AGC) is the topology that is used in this thesis to implement and simulate the sensor. The implementation and simulations are done in 0.35μm XFAB CMOS Process. Since phase noise analyses are readily available in Cadence as Periodic Steady State (PSS), Harmonic Balance (HB) and PNoise Analyses and due to the fact that the obtained phase noise from Cadence, for comparison purposes, can be converted to Allan deviation (as shown in [6]), Phase Noise Analysis is used to evaluate the closed-loop design in CMOS technology.

According to [3], the difference between the phase noise performance of a closed-loop design with an AGC (sinusoidal wave or linear oscillator) and a closed-loop design with a kind of limiter or comparator (square wave or nonlinear oscillator) is that in a loop with an AGC block, the far-from-carrier phase noise (smaller sampling times in Allan deviation) shows much better performance. This comparison is done when the noise is evaluated at the output of the variable gain amplifier in an AGC block or at the output of the comparator. Far-from-carrier phase noise component of square wave oscillator is worse because of the fact that the noise at the input of the limiter or comparator gets modulated in time with the digital behavior of the comparator or limiter before appearing at the output. This kind of noise which arises from the nonlinearity behavior of the comparator or limiter (or digital circuits) is called cyclostationary noise [18]. Cyclostationary noise occurs when the stationary

noise gets modulated by the switching frequency of the comparator. It implies that the noise has a cyclic behavior in time domain. The increase in the phase noise floor by the cyclostationary behavior of noise is also called noise folding. Noise folding is a noise penalty that the input noise sources with the noise bandwidth greater than the bandwidth of modulation get multiplied by [3]. The goal of this thesis is the phase noise floor (far-from-carrier noise) reduction for the sensor implemented in CMOS Technology, therefore square wave topology is not examined in this thesis.

However to be able to manipulate the phase noise floor, parameters that affect the phase noise floor need to be considered in the design. For high quality factor resonators which are operating under low pressure, driving signal level is small, usually smaller than the input common mode range (ICMR) of the electronic circuitry. Power handling capability of the resonator has been defined to address this issue. Power handling capability along with quality factor are important parameters which determine the close-to-carrier and far-from-carrier phase noise components. Beyond the power handling capability of a resonator, the resonator might operate nonlinear or pull-in might happen. Resonators with smaller power handling capability will show higher (worse) far-from-carrier phase noise component due to the fact that the phase noise is the ratio of noise PSD over the signal power at the oscillation frequency. Far-from-carrier phase noise is equivalent to short term instability in Allan deviation - the first biasing slope that appears for smaller sampling times in Allan deviation. It implies that any reduction in far-from-carrier phase noise can be interpreted as reduction in Allan deviation for short term instability. In addition to power handling capability of the resonator, quality factor also determines the Lesson frequency and close-to-carrier phase noise components. Wojciechowski has done a comparison in [3] for far-from-carrier noise component of DETF resonantors in the range of 200 KHz frequencies (Table 1.1). He has shown that the far-from-carrier phase noise for this type of resonator usually might not go beyond -100 dBc/Hz especially when it is functioning under low pressure. He reaches -120 dBc/Hz phase noise for his comb drive DETF resonator by increasing power handling capability of the resonator by driving it in atmospheric pressure. Power handling capability can be improved by increasing coupling factor (increasing the transduction area and reducing the gap between the electrodes) and stiffness of the structure [19].

Table 1.1: Comparison that is done in [3] by Wojciechowski which shows the far-from-carrier phase noise performance of resonators in the range of 200 kHz resonant frequencies.

	Roessig 1997	Nguyen 1999	Seshia 2002	Seth 2004	Wojciechowski 2004
Noise L_{far} [dBc/Hz]	-70	-70	-75	-83	-120
Vacuum	✓	✓	✓	✓	×
Monolithic	✓	✓	✓	×	×
Frequency, f_o	175 kHz	16.5 kHz	145 kHz	57 kHz	217 kHz
Motional Res., R_x	?	3.8 MΩ	?	2.5 MΩ	18 M Ω
Q	17000	51000	10000	14000	370
Amplitude V_{Drive}	?	~ 34 mV	~36 mV	5.3 mV	10 V

In this research, the far-from-carrier (f^0) and f^{-1} phase noise components prediction and reduction are intended to be achieved by using the model that Enrico Rubiola and Wojciechowski offer [3, 6]. Since the designed resonator by Mr. Talha Köse in METU MEMS owns higher quality factor (about 23000), the close-to-carrier phase noise components are expected to have better (small) noise levels if flicker noise of electronic circuitry is designed to be small enough.

1.2 Chapter Organization

This thesis is organized as follows:
Chapter two: The theory of resonant sensors, frequency shift detection methods, characteristics of DETF resonator, front-end amplifiers and their noise and stability analyses, and static and random phase fluctuations in the loop are discussed. Allan Deviation [13] and Phase Noise models based on [6] and [3] are explained.

Chapter three: CMOS based closed-loop design is implemented in this chapter. The simulations and results for the phase noise and transient analysis are represented. All the simulations are done on the extracted layouts.

Chapter four: The design procedure in chapter three is repeated by employing discrete components in the loop. The simulation results and the measurements that are done on the fabricated PCB (Printed Circuit Board) board are represented in this chapter.

Allan deviation is used to evaluate the frequency stability of the closed-loop circuit.

Chapter five: Concludes the study and provides difficulties encountered in the design, it also provides the possible future works and improvements that can be done on the closed-loop design in this research.

CHAPTER 2

THEORY OF RESONANT MEMS SENSORS

The heart of a micro-mechanical resonant sensor, known as the timing element, is a micro-mechanical structure vibrating at its resonant frequency. Output frequency of the sensor is a function of mass and stiffness of the micro-mechanical structure ($\omega_{res} = \sqrt{k/m}$). In other words, any change in the structure which brings about any change in mass or stiffness will drift the resonant frequency. To keep the resonator vibrating at its resonant frequency and make it possible to detect any change in its resonant frequency in response to any change in the quantity to be measured, micro-mechanical resonator needs to be combined with electronics. To accomplish this goal, the resonator is driven by using some kind of excitation technique such as electrostatic, magnetic and thermal, and sensed by some form of detection mechanism like capacitive and piezoresistive. Frequency response of a typical micro-mechanical resonator along with the possible topologies to sustain the vibration and detect any change in the resonant frequency are shown in Figure 2.1. According to the frequency response of a micro-resonator (either amplitude response or phase response), three types of readout circuitry are possible. These frequency shift detection methods are phase, slope and oscillator detection schemes.

Slope and Phase detection schemes, which are functioning based on amplitude and phase changes respectively, have an important disadvantage over Oscillator detection scheme regarding their limited operational bandwidth. Since phase roughly behaves linearly within the bandwidth of the resonator, beyond the bandwidth which is equal to w_0/Q, both methods encounter nonlinearity. Out of the resonator bandwidth, phase enters its nonlinear regime in phase detection method and amplitude drops consider-

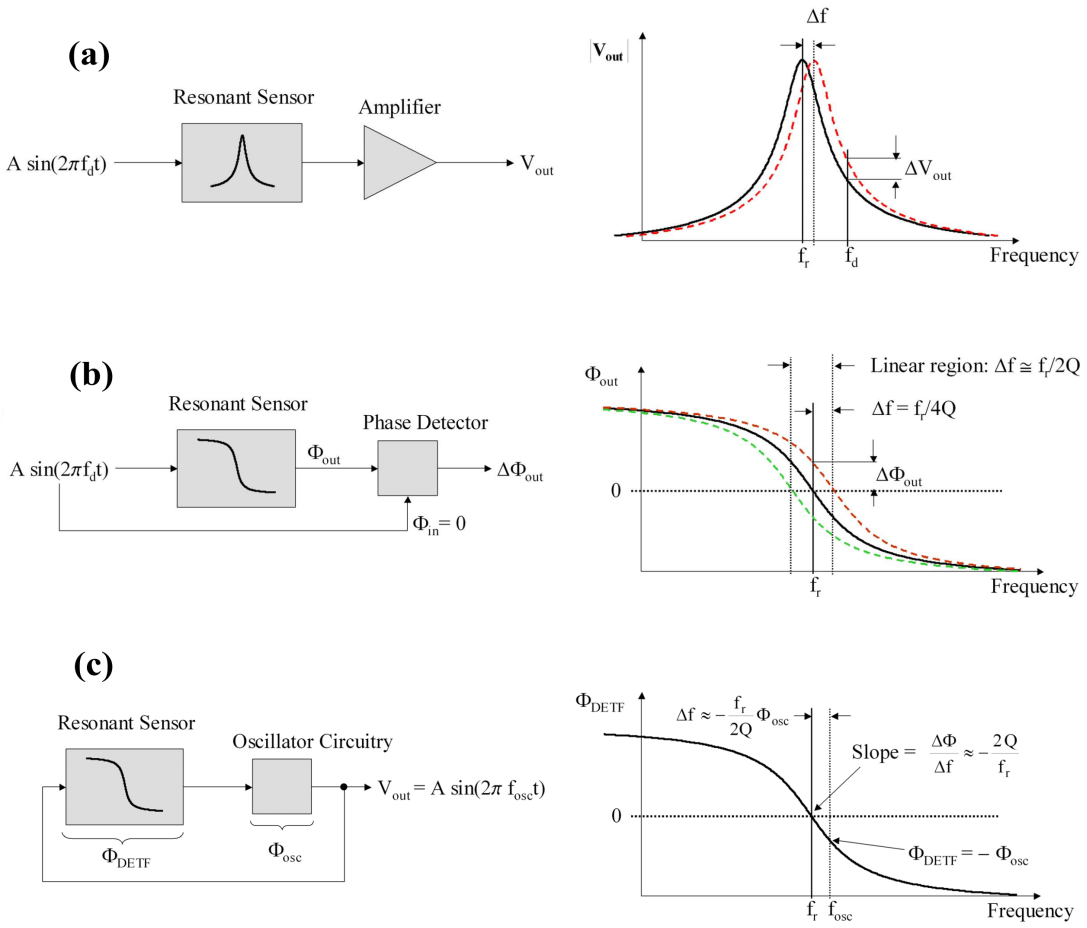


Figure 2.1: Block diagrams of frequency shift detection methods; (a) Amplitude, (b) Phase and (c) Oscillator detection methods [3].

ably in amplitude detection method. It is even worse for low frequency and large quality factor resonators since their bandwidth is much more limited. Small bandwidth makes accurate detection become hard to be achieved in this type of micromechanical resonators. Any change in temperature, pressure inside the package, quality factor of the resonator or proof mass voltage might drift the resonant frequency of the resonator easily. On the contrary, Oscillator detection method does not encounter this problem and is desirable because of the fact that the operating bandwidth will depend on the bandwidth of the electronic circuit.

As a result, the general block diagram of a resonant sensor which takes advantage of the oscillator detection mechanism (closed-loop scheme) for sustaining the oscillation of a resonator and detecting any frequency shift is shown in Figure 2.2.

The closed-loop scheme is comprised of a resonator, a front end amplifier, gain stages

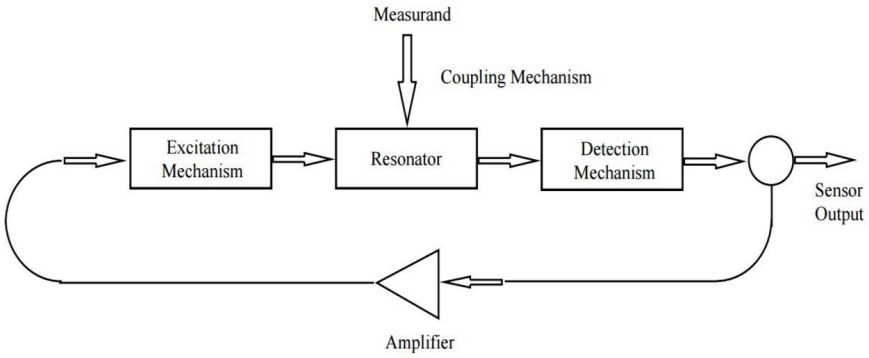


Figure 2.2: Block diagram of a closed-loop circuit (Oscillator) [20].

and if necessary phase shifters. Each one is going to be discussed in the next sections. In addition to these components, some evaluation techniques are required to assess functionality of the oscillator for a specific application, these evaluation techniques characterize the output spectral purity of the oscillator. The evaluation is achieved through either one of the methods in frequency domain (Phase Noise) or in time domain (Allan Deviation). These stability assessment techniques are going to be discussed in this chapter as well.

2.1 Micro-mechanical Resonator

The fundamental geometries for MEMS resonators are cantilever beams, bridges and diaphragms. Bridge is the most commonly used micro-resonator because it is simple to fabricate and operate. It consists of a single beam fixed at both ends. More complicated micro-mechanical resonator geometries, such as double-ended tuning fork (DETF)(Figure 2.3), provide improved performance. These resonators offer dynamically balanced modes of vibration in which the sum of the forces at the anchors, due to the tine motion, is so small. The balanced mode of vibration results in reduced vibration sensitivity and higher quality factor for vacuum encapsulated micro-resonators. It also offers improved long term drift (e.g., aging) due to the fact that the surrounding structure does not participate in the resonator's vibration [20].

Double-ended tuning fork resonator (Figure 2.3) used in this research is driven and sensed symmetrically (out of phase). The resonator is excited and sensed by capaci-

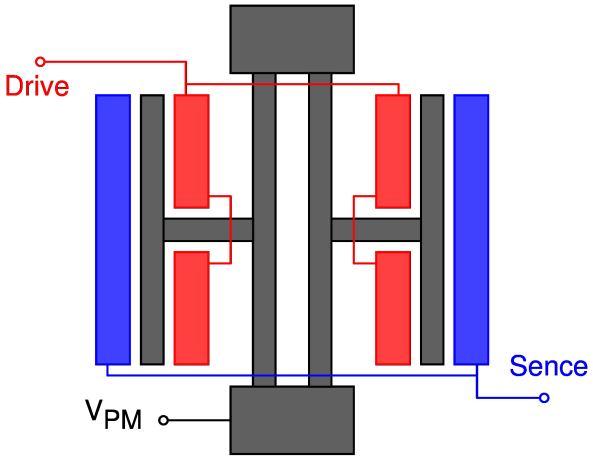


Figure 2.3: DETF resonator - driven and sensed symmetrically.

tive detection mechanism. The electrostatic transduction (capacitive sensing and actuation) is the dominant scheme in MEMS inertial sensors because it is readily available in micro-machining processes. There are other advantages for capacitive sensing and actuation schemes such as low power consumption, low cost and compatibility with IC fabrication technology.

2.1.1 Single-ended Actuation and Balanced Actuation

Actuation and sensing topologies are related to the number and orientation of electrodes which may vary according to different applications. There are two common actuation and sensing topologies for double-ended tuning fork resonators (Figure 2.4): single-ended and balanced actuations. In the single-ended topology, one tine is used for driving the resonator, and the other one is used for sensing. On the other hand, in the balanced actuation (which is employed for the resonator in this study), both tines are driven simultaneously and the motion of both tines are sensed in parallel. The balanced actuation also provides more output signal in comparison with the single-ended topology. Other advantages for the balanced actuation are also mentioned in section 2.1 such as improved long term drift (e.g., aging) and reduction in vibration sensitivity [19].



Figure 2.4: Two common actuation and sensing topologies: balanced (left) and single-ended (right).

2.1.2 Comb-drive Transducer Vs Parallel Plate Transducer

Comb-drive and parallel plate transducers are shown in Figure 2.5. Linearity and signal strength are the key parameters that determine which transducer should be used. For the comb-drive transducer, capacitance is given by



Figure 2.5: Two commonly used transducers are shown in this figure - Comb-drive (left) and Parallel Plate (right).

$$C_{comb} = \varepsilon_0 \frac{Area}{Gap} = \varepsilon_0 \frac{h(l+x)}{g} \tag{2.1}$$

Hence transduction (coupling) factor for the comb-drive transducer is determined by

$$\eta_{comb} = V_P \frac{dC}{dx} = V_P \, \varepsilon_0 \frac{h}{g} \tag{2.2}$$

Which is a constant value. Capacitance for the parallel plate transducer is also obtained by

$$C_{parallel} = \varepsilon_0 \frac{Area}{Gap} = \varepsilon_0 \frac{hl}{(g-x)} \tag{2.3}$$

Consequently transduction factor can be calculated for the parallel plate transducer by (for smaller deflections, $x \ll g$)

$$\eta_{parallel} \;=\; V_P \,\frac{dC}{dx} \;=\; V_P \,\varepsilon_0 \,\frac{hl}{g^2} \tag{2.4}$$

In all the above mentioned equations, h is the thickness of the structure or equivalently is the width of the transduction area, l is the length of the transduction area, g is the gap between the plates, x is the deflection, V_p is the proof mass voltage and ε_0 is the permittivity of free space (8.854$\times$ 10^{-12} Farads/meter). Some of the characteristics of both transduction methods are summarized below:

Comb-drive Transducer - Capacitance in a comb-drive transducer is a function of overlapping area. Due to the large actuation mass in the comb-drive transducer (compared to the parallel plate transducer), sensitivity is smaller. The comb-drive transducer has a smaller dC/dx compared to the parallel plate transducer under the same mass and area conditions. Smaller dC/dx generates smaller electrostatic force hence high voltage is required to actuate a structure with large effective stiffness. However, dC/dx of a comb-drive transducer is constant and independent of position. Therefore the output current is linear and only a function of motion (velocity of the tine).

Parallel Plate Transducer - Capacitance in a parallel plate transducer is a function of gap between the plates. Due to the small actuation mass in the parallel plate transducer (compared to the comb-drive transducer), high sensitivity is achievable. The parallel plate transducer has a larger dC/dx compared to the comb-drive transducer under the same mass and area conditions. Larger dC/dx generates high electrostatic force hence low voltage is required to actuate a structure with large effective stiffness. dC/dx of a parallel plate transducer is not independent of position. Therefore the output current is non-linear.

Maximum deflection, MEMS process constraints, linearity and required voltage or force for actuation are the key factors to choose between parallel plate and comb-drive transducers.

2.1.3 Sensing and Actuation in DETF Resonators

The resonator is excited by electrostatic excitation technique (voltage to force conversion) and sensed by capacitive detection mechanism (motion to current conversion). The relations which exist in electrostatic transducers [21, 22] are represented below. The resonator in Figure 2.3 takes advantage of parallel plate transduction, therefore all the following equations are for this type of transducer.

The stored energy in a capacitor is

$$E \;=\; \frac{1}{2}\, C\, V^2 \tag{2.5}$$

Where V is the potential difference between two plates and C is the position dependent capacitance. It can be shown that for a resonator with f_{res} resonant frequency, if V is chosen to be a pure sinusoidal or square wave with f_{res} fundamental frequency, the stored energy and consequently force between the plates will only have DC portion for square wave (V_{ac}^2) and DC portion plus a $2f_{res}$ term for sinusoidal wave ($V_{ac}^2/4 - (V_{ac}^2/2)\; cos(2\omega_{res}t)$). In order to have a force that contains f_{res} frequency component, a DC term has to be added to the driving sinusoidal or square wave. Doing so, the stored energy, in the case of a sinusoidal driving signal, will be proportional to

$$\begin{aligned} V^2 \;&=\; \Big(V_{DC} - V_{ac}\; sin\big(\omega_{res}t\big)\Big)^2 \\ &=\; \big(V_{DC}^2 + \frac{V_{ac}^2}{2}\big) - 2V_{DC}\; V_{ac}\; sin\big(\omega_{res}t\big) + \frac{V_{ac}^2}{2} cos\big(2\omega_{res}t\big) \end{aligned} \tag{2.6}$$

And in the case of a square wave signal, stored energy will be proportional to

$$\begin{aligned} V^2 \;&=\; \Big(V_{DC} - \frac{4}{\pi} \sum_{n=1,3,5,\ldots}^{+\infty} \frac{V_{ac}}{n}\; sin\big(n\omega_{res}t\big)\Big)^2 \\ &=\; \big(V_{DC}^2 + \frac{2V_{ac}^2}{\pi}\big) - \frac{8V_{DC}\; V_{ac}}{\pi} sin\big(\omega_{res}t\big) + \; Odd\;\; Harmonics \end{aligned} \tag{2.7}$$

The force acting on a parallel plate (Equation 2.3) in the movement direction and the

current achieved from the movement of the tine are given by

- Voltage-to-Force

$$\begin{aligned} F_{drive} &= \frac{dE}{dx} = \frac{1}{2}\frac{dC_d}{dx}\,V^2 \\ &= \frac{1}{2}\left(\varepsilon_0\,\frac{hl}{(g-x)^2}\right)\Bigg(\big(V_{DC}^2+\frac{V_{ac}^2}{2}\big)-2V_{DC}\,V_{ac}\,sin\big(\omega_{res}t\big) \\ &\quad +\frac{V_{ac}^2}{2}cos\big(2\omega_{res}t\big)\Bigg) \end{aligned} \tag{2.8}$$

- Motion (Velocity of the tine)-to-Current

$$\begin{aligned} i_{sense} &= \frac{dQ}{dt} = \frac{d\Big(C_s(t)V_s(t)\Big)}{dt} \\ &= C_s(t)\frac{dV_s(t)}{dt}+V_s(t)\frac{dC_s(t)}{dt} \\ &\approx V_s(DC)\frac{dC_s(t)}{dt} \\ &\approx V_s(DC)\frac{d\Big(C_0+\frac{dC}{dx}x(t)\Big)}{dt} = V_s(DC)\frac{dC}{dx}\times\frac{dx}{dt} \\ &\approx \eta_{sense}\,\frac{dx}{dt} \end{aligned} \tag{2.9}$$

In Equation 2.9, total time-varying capacitance, which is the summation of the stationary and the time-dependent capacitance of the sensing node is expressed as $C_s(t) = C_0 + (dC/dx)x(t)$. Voltage at the sensing node is also expressed as the summation of DC and AC voltages, $V_s(t) = V_s(DC)+V_s(ac)$. AC voltage has been eliminated with this assumption that the DC biasing potential is much larger than the time-varying output voltage. $(dC/dx)\,V_s(DC)$ is the transduction factor. If the transduction factor at the driving node is a larger value, then the produced electrostatic force with respect to the input signal will also be a larger value. The same thing is valid for the sense electrode as well. In addition, since in a trans-impedance amplifier the sensing node

is AC-ground, $V_s(DC)$ is equal to the proof mass voltage of the resonator, V_P.

2.1.4 Equivalent Electrical Model of The Micro-mechanical Resonator (DETF)

In order to achieve the expected results from the micro-mechanical resonator once integrated with the electronic circuitry, the best equivalent electrical model is necessary to be chosen to be simulated in Cadence and LTSpice. How much accurate the model is, more reasonable the final results will be. Even though there might be other parasitics accounting for different phenomena in resonators, it can be sufficient only to use Butterworth Van-Dyke (BVD) model as shown in Figure 2.6. According to this model, a DETF resonator can be represented by a linear mass-spring-damper system. Assuming linearity, a two-port model can be developed and simple equations can be written to describe the structure as shown in [3].

The other method to obtain the electrical model of the resonator is to use a Network Analyzer. The obtained information from the network analyzer can be evaluated as a second order band-pass filter. The RLC filter and its resonance behavior can be described by its quality factor, resonant frequency and peak value. Therefore, Q, ω_{res} and peak value of resonance are measured for the resonator in this method, then they are used to calculate electrical elements as will be shown in section 3.2.1. The key equation used to calculate equivalent electrical elements by a network analyzer is shown below.

$$Quality\ factor = \frac{\omega_{res}}{\Delta\omega} = \frac{1}{R_m C_m \omega_{res}} = \frac{L_m \omega_{res}}{R_m} \tag{2.10}$$

Derived elements by the first method (using equations) are represented by the following equations. Some useful terms are

Young's modulus of silicon	$E = 169 \times 10^9 \quad (Pa)$
Mass density of silicon	$\rho = 2330 \quad (Kg/m^3)$
Permittivity of vacuum	$\varepsilon_0 = 8.854 \times 10^{-12} \quad (F/m)$

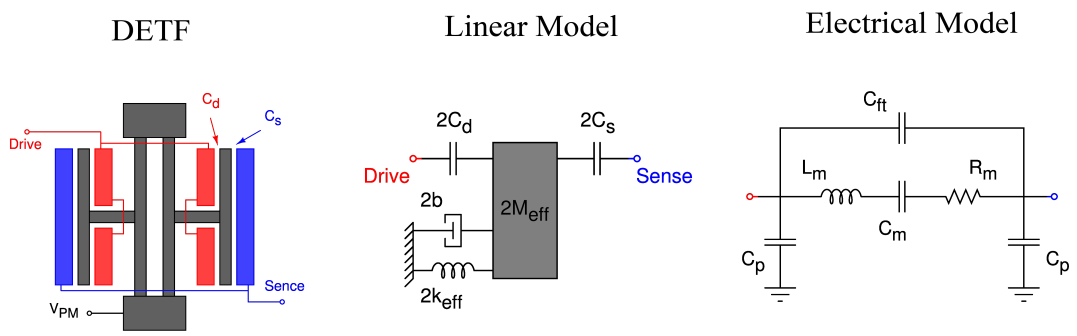


Figure 2.6: Equivalent electrical model of the DETF resonator.

Geometry of the resonator is shown in Figure 2.7.

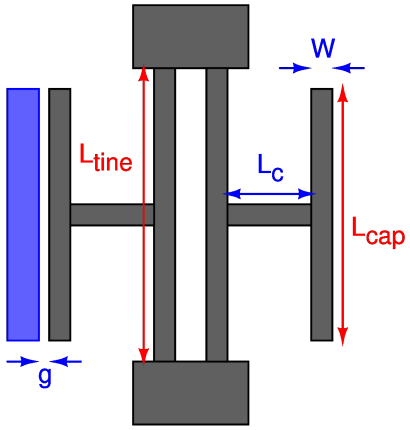


Figure 2.7: Geometry of the DETF resonator is represented in this figure.

By using these dimensions, calculated mass, stiffness, resonant frequency and transduction area are determined by

Transduction Area for one side	$A = L_{cap}h$	(m^2)
Mass	$M = 0.375M_{static} + M_{dynamic} = \rho hg\big(0.375L_{tine} + L_{cap} + L_c\big)$	(Kg)
Stiffness	$k = \big(192EhW^3\big)/\big(12L_{tine}^3\big)$	(N/m)
Resonant frequency	$f_{res} = \sqrt{k/M}$	(Hz)
Coupling Factor	$\eta = V_p\big(\frac{dC}{dt}\big)$	

Finally, equivalent electrical elements for DETF resonator are obtained by

Static capacitance

$$C_p = 2\left(\varepsilon_0 \frac{A}{g}\right) \quad (F) \tag{2.11}$$

Motional resistance

$$R_m = \frac{\sqrt{Mk}}{Q2\eta^2} \quad (\Omega) \tag{2.12}$$

Motional capacitance

$$C_m = \frac{2\eta^2}{k} \quad (F) \tag{2.13}$$

Motional inductance

$$L_m = \frac{M}{2\eta^2} \quad (H) \tag{2.14}$$

η^2 is multiplied by two due to the fact that two sensing and driving capacitors are in the model.

2.1.5 Feedthrough Capacitance in a DETF Resonator

Feedthrough capacitance mainly is due to the gap between the electrodes and the structure (DETF). This parasitic capacitance (Figure 2.6) provides an undesired path for current from input to output electrodes which is called leakage or feedthrough current (I_{ft}). The feedthrough current is due to the carrier charge and discharge between electrodes and the structure even when the structure is not oscillating. If the feedthrough capacitance is larger than the motional capacitance, the sensing current (Figures 2.8 and 2.9) might not reach zero degree. $C_{ft}(max)$ is defined as the maximum feedthrough capacitance in which a resonator reaches zero degree as shown in Figure 2.8. According to [3], $C_{ft}(max)$ is obtained when $I_m = 2 \times I_{ft}$. And for a robust oscillator design, it is required that $C_{ft} = C_{ft}(max)/5$.

At the sensing node, $I_{ft} + I_m$ is equal to I_{sense}. Therefore, if another capacitor is placed in parallel with the feedthrough capacitance and driven with the complementary voltage, the feedthrough current can be canceled. Feedthrough cancellation can be achieved by using an external tunable capacitor or a dummy resonator as shown in Figure 2.9. A dummy resonator can be used in parallel with the original resonator with this difference that no DC biasing voltage is applied to its structure. Therefore the only current flowing through it will be the feedthrough current [23–25]. As a

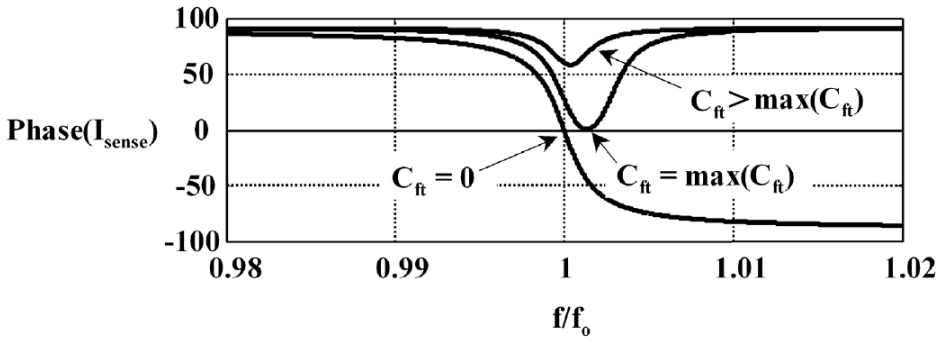


Figure 2.8: Phase shift in the parallel combination of feedthrough capacitance and RLC model [3].

result, two feedthrough currents will cancel out each other and I_m will be the only current flowing through TIA (trans-impedance amplifier).

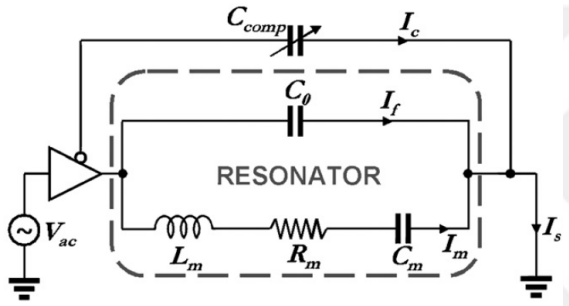


Figure 2.9: Feedthrough cancellation technique using an external variable capacitor [24].

The feedthrough capacitance of the DETF resonator will be measured and calculated in section 3.2. The measurement will be done by a Network Analyzer.

2.1.6 Important Specifications of Micro-resonators

In general, four features of resonators have great influence on the design of an oscillator. These parameters are f_{res} (resonant frequency), R_m (motional series resistance), Q (quality factor of the resonator) and the important one power handling ability [8].

As will be shown in section 2.5.1, f_{res} determines the bandwidth of the TIA amplifier and the whole electronic circuitry. The bandwidth of the sustaining circuitry typically has to be 10 times greater than f_{res} to ensure smaller amount of phase shift in the loop.

R_m determines the electronic circuitry's gain (Ω) and the possible output noise floor

at the steady state. Q also has a bigger role in determining close-to-carrier phase noise (section 2.5.2.5).

Power handling capability is important in MEMS resonator based oscillators. Low power handling capability in a MEMS resonator results in a low amplitude signal in the loop which in turn increases the far-from-carrier phase noise. It will be shown in section 2.5.2.5 that the ratio of noise PSD to the driving signal level at the resonant frequency is a smaller value in resonators with low power handling capability. The power handling capability can be increased by increasing the coupling factor (η) and stiffness.

2.1.7 Nonlinearity (A-f effect in MEMS Resonators)

A-f effect (amplitude-frequency effect) is the dominant nonlinearity source in MEMS resonant sensors [26]. A-f effect occurs because of two kinds of nonlinearities: mechanical and electrical, and it determines some important characteristics of the sensor that are mentioned below:

- Dictates the maximum power which can be handled by the resonator
- Limits short term frequency stability (this parameter is a measure of achievable resolution)
- Causes amplitude to frequency modulation (the frequency of DETF resonator is dependent on its amplitude)

2.1.7.1 Mechanical Nonlinearity (Spring Hardening Effect)

At lower proof mass voltages, as the amplitude increases the tines are forced to extend. This extension in the tines brings additional axial force and consequently the stiffness increases, and so does the resonant frequency. Therefore the stiffness and resonant frequency become signal amplitude dependent. The resonance peak bends toward higher frequencies as the amplitude increases (Figure 2.10(a)).

2.1.7.2 Electrical Nonlinearity (Spring Softening Effect)

At higher proof mass voltages, by increasing amplitude of the driving signal, electrical nonlinearty due to higher electrostatic force makes the effective stiffness of the resonator become smaller and consequently the resonant frequency reduces. It has been shown in [21] that the resonant frequency can be written as $\sqrt{(k_m - \delta k_e)/m}$ if the electrostatic spring effect, δk_e, is taken into account. Unlike mechanical nonlinearity, electrical nonlinearity causes the resonance peak to bend towards lower frequencies by increasing the driving signal (Figure 2.10(b)).

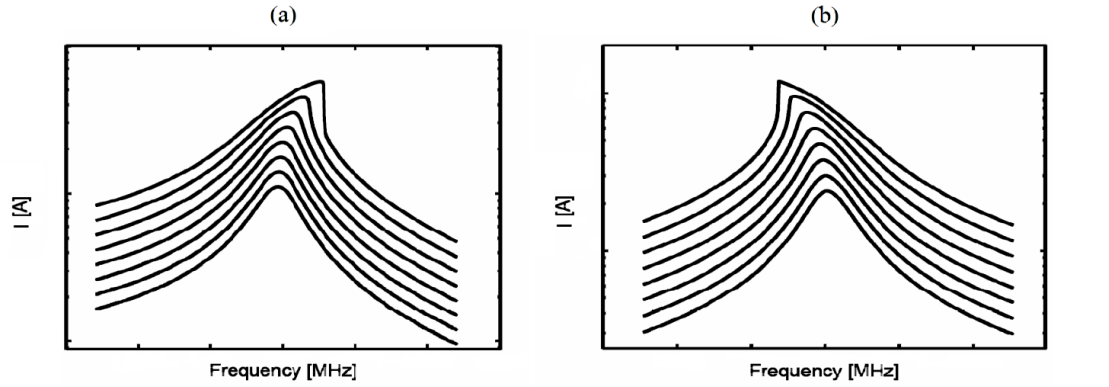


Figure 2.10: Figure above represents (a) mechanical A-f effect (spring-hardening effect) at lower proof mass voltages and (b) electrical A-f effect (spring-softening effect) at higher proof mass voltages [26].

2.2 Front-end Amplifier

2.2.1 Front-end readout circuitry

Since sensing mechanism in this study is capacitive ($q = cv$ and $i = c(dv/dt)$), possible readout circuits can be categorized based on what is sensed; voltage, current or charge. The front-end readout circuitry for current and voltage sources can be implemented by continuous-time (CT) amplifiers, and for charge source can be constructed by discrete-time switch-capacitor (SC) amplifiers (not in the scope of this thesis) [27].

2.2.2 Continuous-time Front-end Amplifiers

Continuous-time amplifiers are categorized into two main groups: Continuous-time Voltage Sensing (CTV) and Continuous-time Current Sensing (CTC) amplifiers. There are different topologies for continuous-time voltage sensing such as Unity Gain Voltage Buffer and Open-Loop Differential Chopper Amplifier. The main disadvantage that a typical CTV amplifier such as Unity Gain Voltage Buffer has in comparison to trans-resistance amplifier is the necessity of a biasing mechanism to stabilize the sensing node (to avoid floating). Another issue with this type of readout circuitry is the sensing node being sensitive to the parasitic capacitance. Due to this fact, if the parasitic capacitance is used to integrate the motional current, the biasing resistor has to be larger than the impedance of the parasitic capacitance. Larger resistor at the input node will rise the output thermal noise of the buffer.

On the other hand, continuous-time current (CTC) sensing amplifiers also known as trans-impedance amplifiers can be considered as parasitic insensitive amplifiers. The biasing for the sensing node is not required for trans-resistance amplifiers because the negative resistive feedback helps biasing the node to a voltage close to zero. The main advantage of CTC amplifiers is being less sensitive to the parasitic in the sensing node (in a case that the operational amplifier has a larger gain); the reason to this fact is the input impedance of a shunt-shunt feedback being equal to the feedback resistor divided by the open-loop gain of the operational amplifier (R_f/A_0).

Trans-impedance amplifiers are categorized as open and closed-loop circuits [28]. Open-loop amplifiers, like common gate (CG) and regulated cascode topology (RGC), first do the current amplification, then by a resistor at the output they achieve current to voltage conversion. They are important because the input resistance is so small. The small input resistance makes them suitable for high frequency applications. On the other hand, noise performance of RGC or CG amplifiers are poor when they are employed to provide higher gains. The poor noise performance is due to the fact that the noise PSD of output resistance will show up at the input. Another drawback of RGC and CG amplifiers is related to the trade off between the gain, which is set by the output resistor, and the voltage headroom at the output node.

On the contrary, closed-loop TIAs are commonly used at low frequency and high motional resistive applications. They are capable of achieving higher gains and better noise performances. Figure 2.11 shows two commonly used TIA topologies. Figure 2.11(b) represents a trans-impedance amplifier with capacitive feedback [29–31] which is frequently used in biomedical applications. It provides very high gains such as $100\ M\Omega$ and avoids dark current (DC current from the input node to the output node). Since high gain is not required for the resonator in this study and to avoid biasing network and DC stabilization at both the input and output nodes, trans-impedance with resistive feedback (trans-resistance) or capacitive feedback (trans-capacitance) is employed(Figure 2.11(a)).

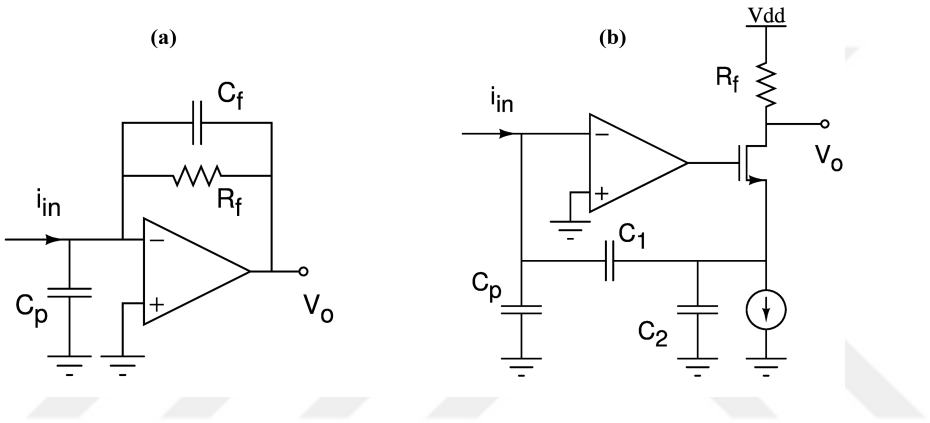


Figure 2.11: Two commonly used TIA topologies are represented in this figure.

2.2.3 Stability and Noise Calculations of a Capacitive or Resistive Feedback Based TIA

Capacitive and resistive feedback based TIAs are used in the CMOS closed-loop circuit design. Obtaining a low noise and a stable amplifier is so critical in the loop in order to keep the noise as small as possible and to avoid any unstability. Regardless of the circuit configuration (TIA, inverting (INV) or noninverting (NI) voltage amplifier) the stability is determined by the complex feedback network which in fact is a voltage divider between the feedback impedance (the output node) and the input impedance (the inverting node)(Figure 2.12) [32–34]. Noise and Stability calculators are also available on [35]. In addition to stability, noise gain bandwidth (NBW) of each noise source is also defined by the components on the feedback network and the

unity gain bandwidth of the operational amplifier.

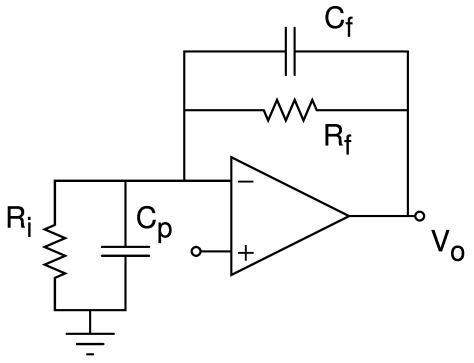


Figure 2.12: Topology used to evaluate stability and noise in TIAs, non-inverting and inverting voltage amplifiers.

These are some useful definitions: Beta (β) is the voltage divided between input impedance on the inverting node and the feedback impedance, and is equal to $Z_i/(Z_f + Z_i)$. Noise-gain (NG) is the gain that the input referred voltage noise, e_n^2, will experience. NG is equal to the non-inverting voltage gain as well.

$$\begin{aligned} NG(S) = \frac{1}{\beta} &= \frac{Z_f + Z_i}{Z_i} = \Big(1 + \frac{R_f}{R_i}\Big)\ \frac{1 + S\big(R_f \parallel R_i\big)\big(C_f + C_i\big)}{1 + SR_fC_f} \\ &= NG(0)\frac{\big(1 + \dfrac{S}{\omega_Z}\big)}{\big(1 + \dfrac{S}{\omega_P}\big)} \end{aligned} \tag{2.15}$$

Zero and pole of the NG, DC Noise Gain (NG_0) and Infinite Noise Gain (NG_∞) are shown in Figure 2.13 and are determined by

$$f_z = \frac{1}{2\pi\big(R_f \parallel R_i\big)\big(C_f + C_i\big)}$$

$$f_p = \frac{1}{2\pi R_f C_f}$$

$$NG_0 = 1 + \frac{R_f}{R_i}$$

$$NG_{\infty} = 1 + \frac{C_i}{C_f}$$

C_p or C_i is the input parasitic capacitance. The natural resonant frequency (f_0) is also given by [32–34]

$$f_0 = \sqrt{GBW \times f_Z} \tag{2.16}$$

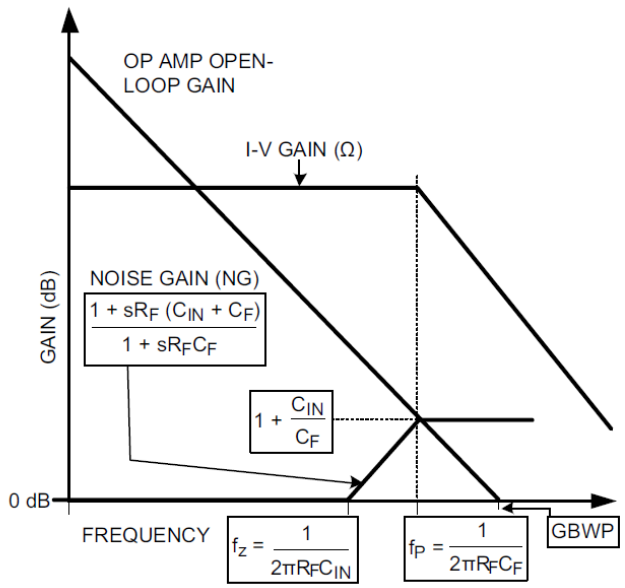


Figure 2.13: Bode plot of a compensated trans-impedance amplifier [36].

2.2.3.1 Stability of a TIA Amplifier

In a TIA configuration, there is no R_i and consequently f_p is greater than f_z. This implies that without the feedback capacitor and its corresponding pole in the noise gain (the zero in the loop gain), there might be about 360 phase shift when noise-gain intersects open-loop gain of the operational amplifier. To prevent this from happening, a feedback capacitor is added in shunt with the feedback resistor in order to produce a pole in the noise gain (a zero in the loop gain). Adding C_f compensates the effect of input pole.

Transfer function of a trans-impedance amplifier is a second order system. To provide a stable loop and adequate phase margin, the proper quality factor for the circuit needs to be chosen. Typically quality factor is selected between 0.5 (critically damped) to 1

(45^o phase margin with small peaking) for trans-resistance amplifiers. In general, the gain and the bandwidth of a TIA are selected first. Then, according to the bandwidth and to the quality factor of the TIA amplifier, C_f is selected. It has been shown in [35] that for the quality factor of 0.5, 0.7 and 1, TIA bandwidths are achieved to be $1.29f_p$, $1.41f_p$ and $1.27f_p$ respectively. f_p, the feedback pole, is equal to $1/(2\pi C_f R_f)$. Thus the proper C_f can be obtained by selecting proper quality factor, bandwidth and R_f in trans-resistance amplifier.

For a trans-capacitance amplifier, the feedback resistor is so large, because of this fact they are usually considered to be overcompensated (quality factors smaller than 0.5) for the operational amplifier with larger unity gain bandwidth product.

2.2.3.2 Noise of a TIA Amplifier

In a CMOS op-amp, the input referred current noise is considered to be very small, thus only two sources of noise will be dominant in a TIA configuration. $v_{R_f}^2$, thermal noise of the feedback resistor, which will appear at the output. And e_n^2, input referred voltage noise of the op-amp, that will contribute to the output voltage noise after being multiplied by the square of the noise gain (Equation 2.17).

$$\begin{aligned}
\overline{v}_{out,rms}^2(TIA) &= \int_0^\infty \Big(e_n^2 \times \big|NG(f)\big|^2 + i_{R_f}^2 \times \big|Z_{TIA}(f)\big|^2\Big)df \\
&= e_n^2 \int_0^\infty \frac{1 + \big(\frac{f}{f_0}\big)^2 \times \big(\frac{f_0}{f_z}\big)^2}{\big(\frac{f}{f_0}\big)^4 + \big(\frac{1}{Q^2} - 2\big)\big(\frac{f}{f_0}\big)^2 + 1} df \\
&\quad + v_{R_f}^2 \int_0^\infty \frac{f_0^2}{\big(\frac{f}{f_0}\big)^4 + \big(\frac{1}{Q^2} - 2\big)\big(\frac{f}{f_0}\big)^2 + 1} df
\end{aligned} \tag{2.17}$$

In [35, 37], the solution for the following normalized integral when $\alpha = 0,\ -2$ is

given by

$$\int_0^\infty \frac{x^{\alpha+2}}{x^4 + \left(\frac{1}{Q^2} - 2\right)x^2 + 1} df = \frac{\pi}{2} Q \tag{2.18}$$

PSD (power spectral density) of e_n^2 in Equation 2.17 is considered to be constant and independent of frequency. That is a reasonable assumption because the contribution of thermal noise to the total output noise is much higher than that of flicker noise. Thermal noise has higher contribution because of the peaking in the noise gain (Figure 2.13). The rms voltage for the output noise can be simplified to

$$\overline{v}_{out,rms}^2(TIA) = e_n^2 \, NG_0^2 \, NBW_{e_n} + v_{R_f}^2 \, NBW_{R_f} \tag{2.19}$$

As shown in [35], noise bandwidth of the feedback resistor is roughly equal to the bandwidth of the TIA. However due to the peaking in the noise gain which is from f_Z to f_P, noise bandwidth for e_n^2 will be equal or greater than GBW of the op-amp. By taking into account the solution to the integral in Equation 2.18 Noise Bandwidth (NBW) for both of the noise sources will be determined by

$$NBW_{R_f} = f_0 \frac{\pi}{2} Q \tag{2.20}$$

$$NBW_{e_n} = f_0 \frac{\pi}{2} Q \left(1 + \frac{GBW}{f_z}\right) \tag{2.21}$$

For a TIA, $NG_0 = 1$ and $f_P \ll GBW$. The final result for the output voltage noise is given by

$$\overline{v}_{out,rms}^2(TIA) = e_n^2 \, f_0 \, \frac{\pi}{2} Q \left(1 + \frac{GBW}{f_z}\right) + v_{R_f}^2 f_0 \frac{\pi}{2} Q \tag{2.22}$$

C_i in a TIA is larger than C_f that increases the NBW of e_n^2. Thereby in order to decrease noise bandwidth, reduction of C_i is necessary.

2.2.3.3 Noise and Stability of NI and INV Voltage Amplifiers

For non-inverting and inverting voltage amplifiers, noise and stability calculations follow the same procedure. However, in NI and INV amplifiers, R_i is usually smaller than R_f which will move f_Z of the NG above f_P and as a result there will not be any gain peaking in the noise gain. Additionally, if f_Z and f_P are chosen to be smaller than GBW of the operational amplifier, the effect of noise at higher frequencies will be reduced.

2.3 DETF Resonator Integrated with a Trans-impedance Amplifier

DETF resonator and trans-impedance amplifier have been discussed in the previous sections. As shown in [21, 22], the integration of DETF resonator and TIA comes in handy in the simulations such as PI parameters estimation for an AGC block. Thus the transfer function of their integration is given in Equation 2.23. The transfer function is obtained by using equations from section 2.1.3.

$$\begin{aligned}
\frac{V_{out}(tia)}{V_{in}(detf)}(s) &= \frac{F_{drive}}{V_{in}(detf)} \times \frac{X}{F_{drive}} \times \frac{I_{sense}}{X} \times \frac{V_{out}(tia)}{I_{sense}} \\
&= \left(V_{PM}\,\frac{dC_{drive}}{dx}\right)\left(\frac{(1/m)}{s^2 + (\omega_{res}/Q)\,s + \omega_{res}^2}\right) \\
&\quad \times \left(V_{PM}\,\frac{dC_{sense}}{dx}\,s\right)\left(R_f \parallel \left(\frac{1}{C_f s}\right)\right) \\
&= \left(\eta_{drive}\right)\left(\frac{(1/m)}{s^2 + (\omega_{res}/Q)s + \omega_{res}^2}\right) \\
&\quad \times \left(\eta_{sense}\,s\right)\left(R_f \parallel \left(\frac{1}{C_f s}\right)\right) \\
&= \frac{\eta_{drive}\eta_{sense}(1/m)s}{s^2 + (\omega_{res}/Q)s + \omega_{res}^2}\left(R_f \parallel \left(\frac{1}{C_f s}\right)\right)
\end{aligned} \tag{2.23}$$

2.4 Closed-Loop Topologies

Three typical oscillator topologies [38, 39] are shown in Figure 2.14. The first topology is an oscillator with no limiter (Figure 2.14(a)). There is only a comparator to drive the resonator. The amplitude limiting is done by the resonator itself which is not desirable in most applications. Nonlinear behavior of the resonator provokes new close-to-carrier phase noise components that are not desirable from sensor resolution point of view. The other two topologies (Figure 2.14(a) and (b)) have superior performance because they take advantage of some sort of limiting technique before driving the resonator. The Barkhausen criterion needs to be satisfied to reach an oscillation in all the topologies. At the start-up, the loop gain has to be more than one to guarantee a quick rising and at the steady state, the loop gain needs to be unity. In both modes, phase shift in the loop must be equal to zero ($\Delta\phi_{loop} = 0$). Phase noise performance of topologies with an AGC block and a limiter (Figure 2.14(a) and (b)) will be examined at the end of this chapter.

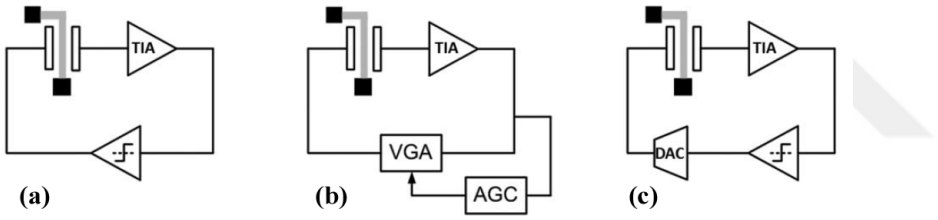


Figure 2.14: Three main oscillator topologies: (a) hard limiter based oscillator, (b) AGC based oscillator and (c) clamped limiting based oscillator are shown in this figure [38, 39].

2.4.1 Tuning Range and Relaxation Time of an Oscillator

The general block diagram for an oscillator is shown in Figure 2.15 which will be used to evaluate phase noise in the next sections. β is an ideal resonator and A is the electronic circuitry. The oscillator tuning range (Figure 2.15) is defined as the frequency range in which $|A\beta(\omega)| > 1$. In this region, the amplitude can be stabilized by an AGC (automatic gain control) block or by a limiter, and the phase determines the oscillation frequency. Out of this range, the response to a perturbation decays exponentially, therefore no oscillation is possible.

Another important parameter of an oscillator is the resonator relaxation time which is

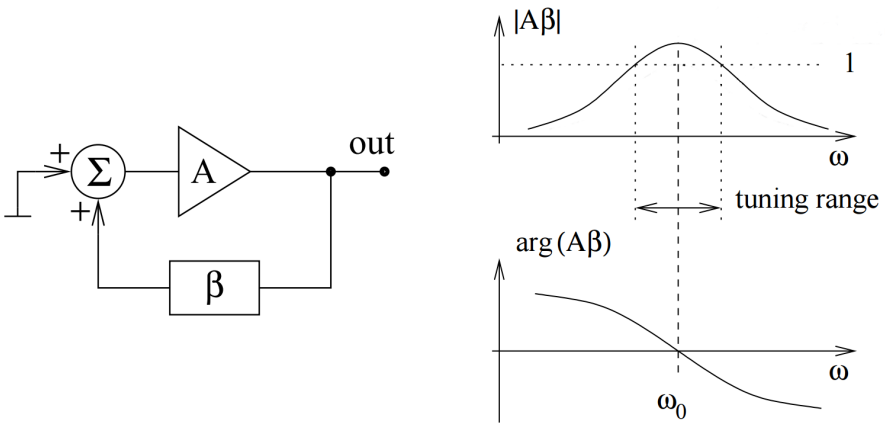


Figure 2.15: The general block diagram of an oscillator. β is an ideal resonator and A is the electronic circuitry.

given by

$$\tau = \frac{Q}{\pi f_{res}} = \frac{2Q}{\omega_{res}} \tag{2.24}$$

It is the time constant defined for a second order low pass filter. It can also be obtained from the resonator bandwidth as well. Reciprocal of that is known as Leeson frequency will be used to examine any phase noise to frequency noise conversion in the closed-loop circuit (Equation 2.26).

2.5 Static and Random Phase Shift in the Loop

Two types of phase shifts are possible in the loop; static phase lag or lead introduced by the electronic circuitry, which is going to be discussed in the next section, and random phase shift that is going to be examined in the section regarding phase noise.

2.5.1 Phase Shifter

Electronic circuitry generally will introduce a static phase lag, ψ, in the loop, as shown in Figure 2.16. If no phase shifter is used in the loop to compensate the phase error, the oscillator will lock itself to a frequency which makes the phase change in the loop to be equal to zero, $\Delta\phi_{loop} = 0$. In other words, as long as we are in the tuning range, phase will determine the oscillation frequency and it will lock the oscillator to a frequency smaller than resonant frequency of the resonator.

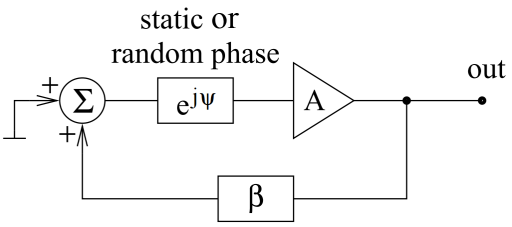


Figure 2.16: Any static or random phase shift introduced in the loop is shown in this figure [15].

Figure 2.17 represents a case in which a static phase lead is introduced by the electronics. As a result, the oscillator will be pulled to a higher frequency.

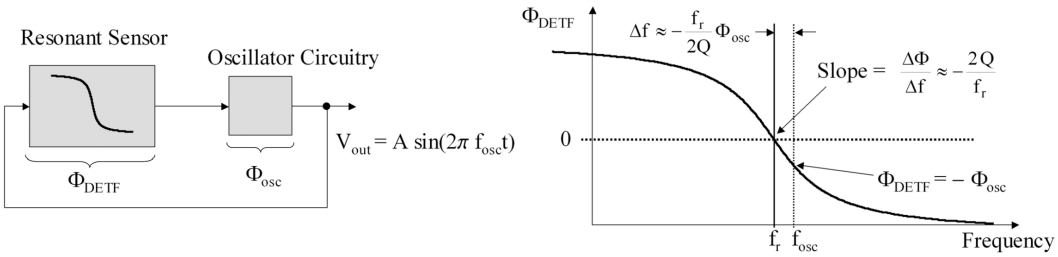


Figure 2.17: Static phase lead in the loop is introduced and the oscillator will be pulled to a higher frequency (higher than natural resonant frequency of the resonator) [3].

The obvious drawback that a large static phase shift might bring up in an oscillator (with high quality factor) is that the motional resistance will be increased and further gain stages might be required to compensate that. Additional gain stages in the loop may heighten noise floor at the output of the oscillator. Increased thermal noise, as will be shown in the next sections, will increase far-from-carrier phase noise component (noise floor) for the same output signal power. Thus, working in the $3dB$ bandwidth is desirable due to the fact that it avoids further gain stages in the loop. As a result, the total bandwidth of the electronic circuitry in the loop is typically chosen to be at least 10 times the resonant frequency of the resonator. This is done to guarantee that the oscillator will operate in the resonator bandwidth and also smaller phase shifting occurs by the electronic circuitry.

The frequency shift in resonator with respect to any static phase shift in the loop

is given by Equation 2.27 (which is valid within the bandwidth of the resonator). Equation 2.27 is obtained by taking derivative of the resonator phase equation in the vicinity of the resonant frequency, f_{res}. ϕ_{osc} is the phase shift introduced by the electronic circuitry and f_{osc} is the frequency of the oscillation.

$$\frac{d}{d\omega}\Big(arg\beta(\omega)\Big) = -\frac{2Q}{\omega_{res}} \tag{2.25}$$

$$\Delta f = -\frac{f_{res}}{2Q}\,\Delta\phi \tag{2.26}$$

$$f_{osc} = f_{res} - \Delta f = f_{res}\Big(1 + \frac{\Delta\phi}{2Q}\Big) \tag{2.27}$$

Since the case study for this research is a temperature sensor, Equation 2.27 will be used to calculate temperature coefficient of the electronic circuitry in chapter three.

2.5.2 Stability Evaluation by Phase Noise (PN) and Allan Deviation (ADEV)

2.5.2.1 Phase Noise of an Oscillator or a Two Port Amplifier

The static phase in Figure 2.16 can be replaced with a random phase fluctuation, $\psi(t)$, that accounts for all the phase noise sources in the loop. Equation 2.28 represents the output of a sinusoidal oscillator. $\phi(t)$ in this equation is the phase noise in the output signal. In the following sections, Enrico Rubiola's model [6] which is based on Leeson's equation will be examined. In a nutshell, he expresses how $\psi(t)$ (phase noise in the open-loop electronic circuitry) is converted to $\phi(t)$ (phase noise in the closed-loop or phase noise at the output of the oscillator). After analyzing what Leeson's equation offers, phase noise calculations for sinusoidal and square wave closed-loop circuits are carried out by following the work that is done in [3].

$$v(t) = V_0 cos\Big(\omega_{res}t + \phi(t)\Big) \tag{2.28}$$

Oscillators operating at steady state condition, take advantage of some sort of amplitude controlling mechanism in the loop to avoid any kind of nonlinearity in the

oscillation signal and to make oscillation amplitude stable. This means that phase noise predominates and therefore amplitude noise is often ignored.

In addition to oscillators, phase noise exists for two port devices such as operational amplifiers as well. According to [6], in a typical case, the amplifier phase noise contains thermal noise (f^0) and flicker noise (f^{-1}). They both have a Guassian PDF (probability density function) and averaging each one results in a specific mean value. The thermal noise portion of the phase noise is dependent on the signal power while the f^{-1} portion is not signal power dependent. On the contrary, some of noise sources with steeper slopes (e.g., random walk) do not exist in the output of an operational amplifier since with their existence group delay will never converge, this never happens in a real operational amplifier. These steeper noise sources are non-statinary [16], it means that through sampling and averaging, their mean values will never converge (Figure 2.18). This is the reason why Allen deviation or modified Allen deviation are used instead of standard deviation to evaluate stability in an oscillator (phase or frequency fluctuation). Noise sources such as random walk frequency and frequency drift exist in oscillators not in two port devices like operational amplifiers. Standard Deviation can not converge for these non-stationary noise sources because their mean values are drifting. Standard Deviation subtracts total mean value from each sample. However, Allen deviation averages two or more adjacent data samples before squaring, summing and averaging.

It has been shown by Behzad Razavi in [40] that "the PDF (probability density function) and PSD (power spectral density) generally bear no relationship". It implies that the PSD profile generally does not say anything about the PDF. For instance, thermal noise has a white PSD and is Gaussian. On the other hand, flicker noise has a frequency dependent PSD, but still it has a Gaussian PDF.

2.5.2.2 Phase Fluctuation Evaluation by Frequency or Phase Noise (In Frequency Domain) or Fractional Frequency (In Time Domain)

In general, any fluctuation in the instantaneous phase of Equation 2.28, $\omega_{res}t + \phi(t)$, can occur due to noise, temperature, aging and etc. These terms that bring about uncertainty in phase or frequency are categorized as short and long term stabilities and

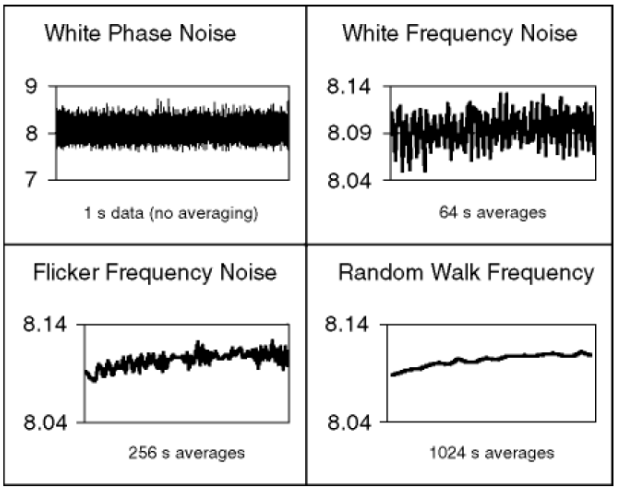


Figure 2.18: An example of noise averaging from [16].

are examined by Phase Noise (PN) in frequency domain and Allan Deviation (ADEV) in time domain. Long term stability of a signal addresses how the signal varies over a long term for example hours and days. Short term stability of a signal source addresses the variations that take place over a shorter period for instance smaller than a second.

Since phase and frequency are convertable to each other, phase noise can be evaluated by observing both phase noise PSD ($\phi(f)$) or frequency noise PSD (also called resolution per Hz) $f^2\phi(f)/f_{res}^2$. Phase noise is the noise, arising from the short term phase fluctuations occurring in a signal. The fluctuations appear as sidebands which spread out either side of the signal.

Fractional frequency, $y(t) = \Delta f/f_{res}$, is also used to measure the frequency fluctuation in time domain. It is measured by comparing the zero crossings between the designed sensor and a reference oscillator in the time domain. Allan deviation uses the data collected from this comparison and predicts deviation from the nominal resonant frequency. It also finds the suitable averaging time which makes it possible to get rid of white phase, flicker phase and white frequency noise sources by averaging.

Power laws for Allan variance, phase and frequency spectra are shown in Figure 2.19. Table 2.1 provides some conversion formulas to calculate ADEV from frequency noise PSD. As shown in [6, 12], Allan variance can always be calculated from frequency PSD, but the inverse is not free from errors. Table 2.1 represents noise types,

their PSDs and Allan variance. This table can be used to convert phase noise obtained from Cadence to Allan variance.

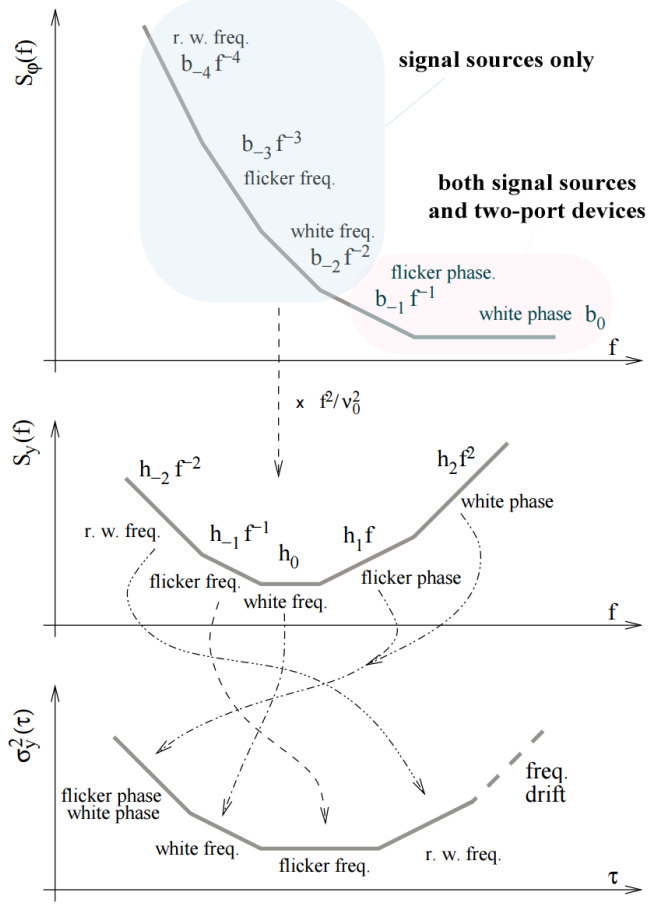


Figure 2.19: Noise types, their PSDs and Allan variance are shown in this figure [12].

Table 2.1: This table represents noise types, their PSDs and Allan variance [6].

noise type	$S_\varphi(f)$	$S_y(f)$	$S_\varphi \leftrightarrow S_y$	$\sigma_y^2(\tau)$	$\mathrm{mod}\,\sigma_y^2(\tau)$
white φ	b_0	$h_2 f^2$	$h_2 = \frac{b_0}{\nu_0^2}$	$\propto \tau^{-2}$	$\propto \tau^{-3}$
flicker φ	$b_{-1} f^{-1}$	$h_1 f$	$h_1 = \frac{b_{-1}}{\nu_0^2}$	$\propto \tau^{-2}$	$\propto \tau^{-2}$
white f	$b_{-2} f^{-2}$	h_0	$h_0 = \frac{b_{-2}}{\nu_0^2}$	$\frac{1}{2} h_0 \tau^{-1}$	$\frac{1}{4} h_0 \tau^{-1}$
flicker f	$b_{-3} f^{-3}$	$h_{-1} f^{-1}$	$h_{-1} = \frac{b_{-3}}{\nu_0^2}$	$2\ln(2)\ h_{-1}$	$\frac{27}{20}\ln(2)\ h_{-1}$
rand. walk f	$b_{-4} f^{-4}$	$h_{-2} f^{-2}$	$h_{-2} = \frac{b_{-4}}{\nu_0^2}$	$\frac{4\pi^2}{6} h_{-2} \tau$	$\frac{4\pi^2}{6} h_{-2} \tau$

Phase noise measurement is available in Harmonic Balance (HB), Periodic Steady State (PSS) and PNoise Analyses in Cadence. Hence CMOS readout circuitry design is done based on phase noise and what Leeson's equation offers. However for the closed-loop circuit with discrete components, Allan deviation is used to evaluate the resolution and stability.

2.5.2.3 Phase Noise Measurement

Phase Noise is measured by a Spectrum Analyzer or using Phase locked loop method. The main drawback of using Spectrum Analyzer to measure PN is that it generally measures the noise in the sidebands that extend out either side of the carrier. The measurement is actually a measurement of $V^2(f)$ and not $\phi^2(f)$. In other words it measures the summation of the phase noise and amplitude noise [11]. In contrast with the previous method, Phase locked loop (Figure 2.20) provides better results for the phase noise measurement [41, 42]. Signals from the oscillator under test and the reference oscillator are applied to the saturated inputs of the mixer [43] and are mixed 90 degrees out of phase. Hence short term phase fluctuations ($\phi(f)$) between two oscillators will appear as voltage fluctuation ($V(f)$) at the output of the mixer as shown in Figure 2.20. k_ϕ is the phase detector gain.

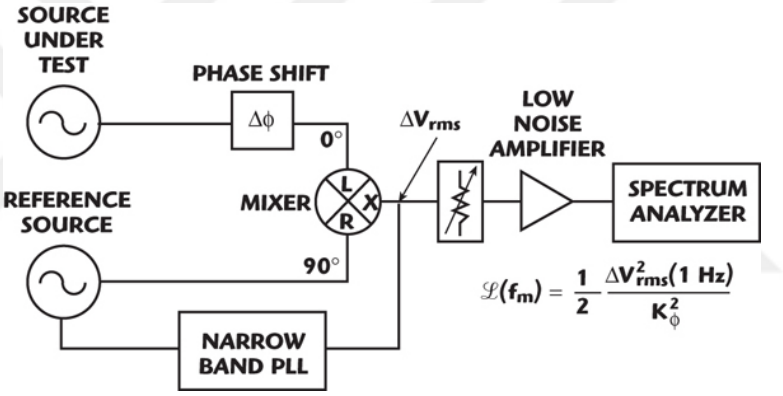


Figure 2.20: Phase noise measurement by using a PLL [44].

2.5.2.4 Sensor Resolution and Frequency Resolution

Resolution of a DETF sensor [3] is defined as

$$Sensor\ resolution\ = \frac{frequency\ resolution}{sensitivity\ of\ the\ sensor} = \frac{\sqrt{\int f_m^2\ \phi(f_m)\ df_m}}{\frac{df}{d(Quantity)}} \quad (2.29)$$

Sensitivity of the sensor is dominated by the resonator sensitivity to the quantity (to be measured). Electronic circuitry usually has the smallest effect on the sensitivity. The other parameter to improve the resolution of the sensor (minimum detectable

quantity change) is the frequency resolution (minimum detectable frequency change) of the sensor. It can be done by reducing phase noise or frequency noise.

2.5.2.5 Phase Noise (Leeson's Equation)

According to Leeson's equation (Equation 2.35), stability can be examined in two different sections; close-to-carrier and far-from-carrier phase noise components as shown in Figure 2.21. The impact of electronic circuitry on each part are discussed below based on both Enrico Rubiola's description of the Leeson effect [6] and K. E. Wojciechowski's work [3].

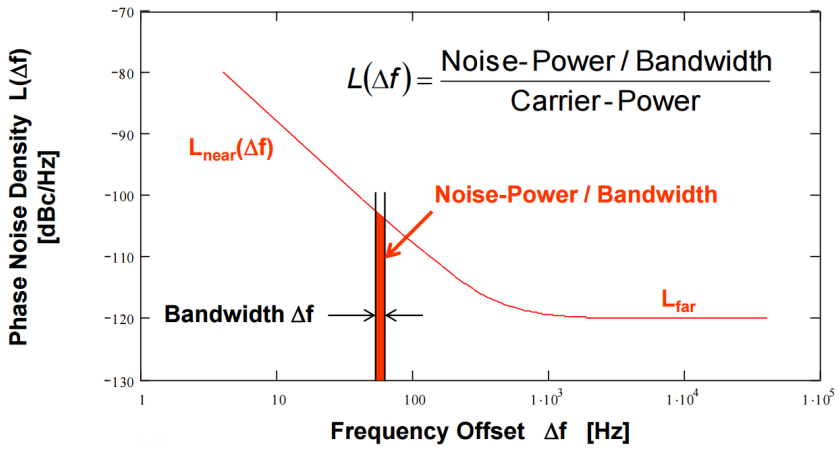


Figure 2.21: Phase Noise (dBc/Hz) [45].

It has been discussed that the $\phi(t)$ (phase fluctuations at the output of the sensor) is the effect of $\psi(t)$ (open-loop phase fluctuations). Enrico Rubiola analyzes a mechanism in which the power spectrum density of ψ is transferred into ϕ. There will be two types of behaviors: slow and fast components of $\psi(t)$ - slower and faster than the inverse of the relaxation time. For the slower components of $\psi(t)$, $\psi(t)$ can be treated as quasi-static perturbation. Hence (from Equation 2.26)

$$\Delta f = \frac{f_{res}}{2Q}\,\psi(t) \tag{2.30}$$

and

$$S_{\Delta f}(f) = \left(\frac{f_{res}}{2Q}\right)^2 S_{\psi}(f) \tag{2.31}$$

The instantaneous output phase is determined by

$$\phi(f) = 2\pi \int (\Delta f) df \tag{2.32}$$

The time-domain integration is expressed by a multiplication by $1/j\omega$ in the Fourier transform domain. Hence, it also maps into a multiplication by $1/(2\pi f)$ in the spectrum. Consequently, the oscillator spectrum density for the slower components of $\psi(t)$ is given by

$$S_\phi(f) = \frac{1}{f^2} \left(\frac{f_{res}}{2Q} \right)^2 S_\psi(f) \tag{2.33}$$

For the fast fluctuations of ψ, faster than the inverse of the relaxation time, loosely speaking, the loop is considered open circuit [6]. The fluctuations in $\psi(t)$ cross the amplifier and show up at the output, without being fed back at the electronic circuitry input. No noise regeneration occurs in this condition, thus $\phi(t) = \psi(t)$, and

$$S_\phi(f) = S_\psi(f) \tag{2.34}$$

Under the assumption that there is no correlation between slow and fast fluctuations [6], Equations (2.33) and (2.34) can be added.

$$S_\phi(f) = \left[1 + \frac{1}{f^2} \left(\frac{f_{res}}{2Q} \right)^2 \right] S_\psi(f) \tag{2.35}$$

The above formula (Leeson equation) can be rewritten as

$$S_\phi(f) = \left[1 + \left(\frac{f_L^2}{f^2} \right) \right] S_\psi(f) \tag{2.36}$$

where

$$f_L = \frac{f_{res}}{2Q} = \frac{1}{2\pi\tau} \tag{2.37}$$

is the Leeson frequency. The formula (2.35) was originally proposed by David B. Leeson as a model for short-term frequency fluctuations. By inspection on Equation 2.36, the closed-loop behavior is that of a first-order filter with an integrator (a

pole in the origin) and a 3dB cutoff frequency of f_L (a zero on the real left axis) as represented in Figure 2.22. Its time constant is the relaxation time, τ, of the resonator.

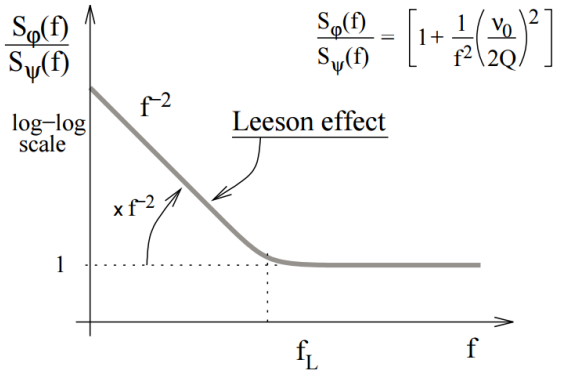


Figure 2.22: The Leeson effect transfer function (the open-loop phase fluctuations to the closed-loop phase noise).

Equation 2.35, and equivalently Equation 2.36 account only for the phase-to-frequency conversion in the loop. The resonator noise is not included in the noise spectrum. In conclusion, the Leeson effect multiplies amplifier phase noise spectrum below the Leeson frequency, $f_L = f_{res}/2Q$, by f^{-2}. As shown in Figure 2.22, if the phase noise of the open-loop circuitry, $S_\psi(f)$, is known, then the phase noise of the oscillator, $S_\phi(f)$, can be predicted. Figure 2.23 also represents two different phase noise profiles for the output phase noise of an oscillator. For a resonator with high quality factor and low resonant frequency like the one used in this study ($f_{res} = 174.818KHz$ and $Q = 23000$), Leeson frequency is smaller than corner frequency of the electronic circuitry, therefore type 2 in Figure 2.23 is the output phase noise predicted for the resonator.

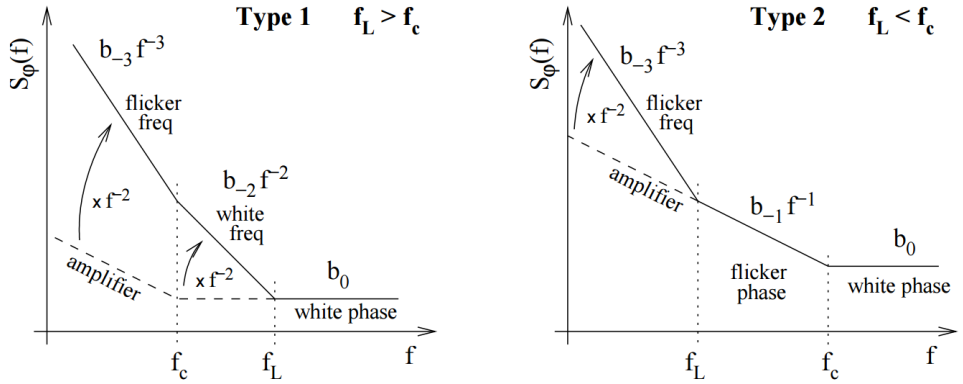


Figure 2.23: The Leeson effect - typical oscillator [6].

2.5.3 Phase Noise Derivation by Employing Wojciechowski's Method

2.5.3.1 Phase Noise of a Sinusoidal Wave Oscillator (Linear Oscillator)

Phase noise can be derived for the closed-loop circuit by the same method that is represented in [3]. The circuit diagram of the closed-loop along with the noise sources are shown in Figure 2.24.

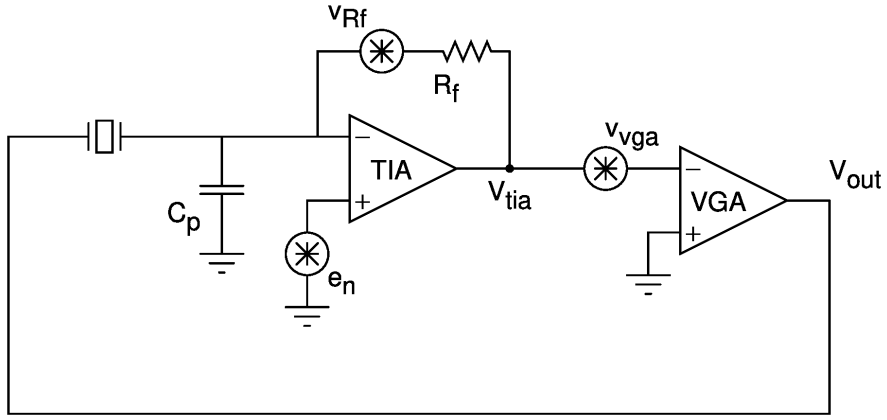


Figure 2.24: This figure represents the circuit diagram of an oscillator along with the noise sources in the loop.

The loop gain, $A\beta$, is determined by

$$A\beta(s) = \frac{\frac{\omega_{res}}{Q}s}{s^2 + \frac{\omega_{res}}{Q}s + \omega_{res}^2} \tag{2.38}$$

Equation 2.38 is obtained at the steady state when $R_f \times A_{vga}$ is equal to R_m. In this equation, R_m is the motional resistance of resonator, R_f is the gain of the trans-impedance amplifier, A_{vga} is the gain of the VGA at the steady state condition when the loop gain is one, e_n is the input referred voltage noise of the operational amplifier, v_{R_f} is the thermal noise of the feedback resistor and finally v_{vga} is the input referred voltage noise of the variable gain amplifier. Because of the fact that Figure 2.24 represents a positive feedback loop, if all the noise sources are referred to V_{tia} (output node of the TIA amplifier), the output referred voltage noise of the closed-loop circuit can be written as

$$\begin{aligned} \overline{v}_{out}^2 &= \left|\frac{-A_{vga}}{1-A\beta}\right|^2 \overline{v}_{tia}^2 \\ &= A_{vga}^2 \left|\frac{s^2+\frac{\omega_{res}}{Q}s+\omega_{res}^2}{s^2+\omega_{res}^2}\right|^2 \overline{v}_{tia}^2 \end{aligned} \tag{2.39}$$

$s = j\omega$ is replaced with $s = j(\omega_{res} - \omega_m) = j2\pi(f_{res} - f_m)$. f_m is the offset frequency from the resonant frequency. For small deviations of f_m, Equation 2.39 can be rewritten as

$$\overline{v}_{out}^2(f_m) = A_{vga}^2 \left(1 + \left(\frac{f_{res}}{2Qf_m}\right)^2\right) \overline{v}_{tia}^2 \tag{2.40}$$

$A_{vga}^2 \times \overline{v}_{tia}^2$ is the open-loop output noise which has been multiplied by the phase noise transfer function, $1 + (f_{res}/2Qf_m)^2$. This transfer function has been obtained by Equation 2.35 as well. Output noise of the open-loop circuitry will have thermal noise and flicker noise PSDs and it could be rewritten as

$$\overline{v}_{out}^2(f_m) = A_{vga}^2 \left(1 + \left(\frac{f_{res}}{2Qf_m}\right)^2\right) \left(1 + \frac{f_c}{f_m}\right) \overline{v}_{th}^2 \tag{2.41}$$

As shown before, in a case that corner frequency, f_c, is larger than Leeson frequency, f_L, phase noise will contain only f^0, f^{-1} and f^{-3}, and some other steeper components such as random walk of frequency. According to the definition, phase noise can be expressed as the ratio of noise PSD over signal power at the resonant frequency as represented below

$$S_\phi(f_m) = \frac{\overline{v}_{out}^2(f_m)}{v_{osc}^2(rms)} = \frac{A_{vga}^2}{v_{osc}^2(rms)} \left(1 + \left(\frac{f_{res}}{2Qf_m}\right)^2\right) \left(1 + \frac{f_c}{f_m}\right) \overline{v}_{th}^2 \tag{2.42}$$

2.5.3.2 Phase Noise of a Square Wave Oscillator (Non-linear Oscillator)

Phase noise calculations for a square wave oscillator is represented in [3] as well. In this work, especially thermal noise behavior in a closed-loop with some kind of nonlinearity (e.g., comparator) is analyzed (Figure 2.25). Wojciechowski shows the nonlinear behavior of the square wave oscillator in Figure 2.26.

Noise at the input of the comparator is amplified by the gain at the rising and falling edges of the output signal. However for the rest of the time that the comparator output is saturated, there will not be any amplification of the noise. As a result, due to this behavior of the comparator, noise will be cyclic at the output. This type of noise is called cyclostationary noise [18]. This amplified noise is also described by the noise penalty in [3].

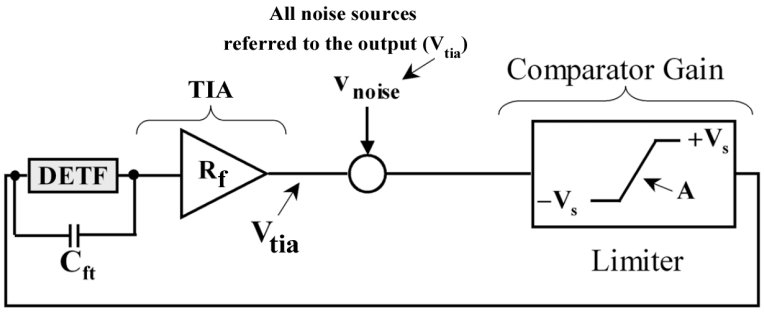


Figure 2.25: Circuit diagram of a closed-loop circuit which takes advantage of some sort of limiter instead of a variable gain amplifier.

As also shown in Figure 2.26, a periodic signal with period T can be represented by the summation of its frequency components (its Fourier series coefficients, x_n). The total power in time domain, is the sum of the power in each x_n in frequency domain. Therefore, the noise penalty [3] is represented by

$$\gamma = \sum_{n=-\infty}^{+\infty} |x_n|^2 \approx \sum_{n=-\infty}^{+\infty} \left| sinc\left(\frac{A_L}{2A}\right) \right|^2 \tag{2.43}$$

A is the gain that the noise experiences at the rising and falling edges of the square wave and A_L is the gain that makes the loop gain become unity, $A_L = R_m/R_f$. Wojciechowski says noise sources with smaller noise bandwidth, much smaller than

$2f_{res}$ will be at the output without getting multiplied by the noise penalty. However noise sources with larger noise bandwidths, are multiplied by the noise gain at the output. This phenomenon is also called as the noise folding.

2.6 Conclusion

Two different phase noise evaluation methods are discussed in this chapter. The difference between them is related to the dependency of f^{-1} phase noise component on the signal power. According to [6], f^{-1} phase noise component is not dependent on the signal power while in [3] all the noise sources are scaled up by the signal power at the oscillation frequency. Additionally, it has been shown in the previous sections that the closed-loop circuit with an automatic gain control block has a superior performance from far-from-carrier phase noise point of view. Therefore, as the amplitude limiting technique, AGC is employed in the closed-loop design in CMOS technology in the next chapter.

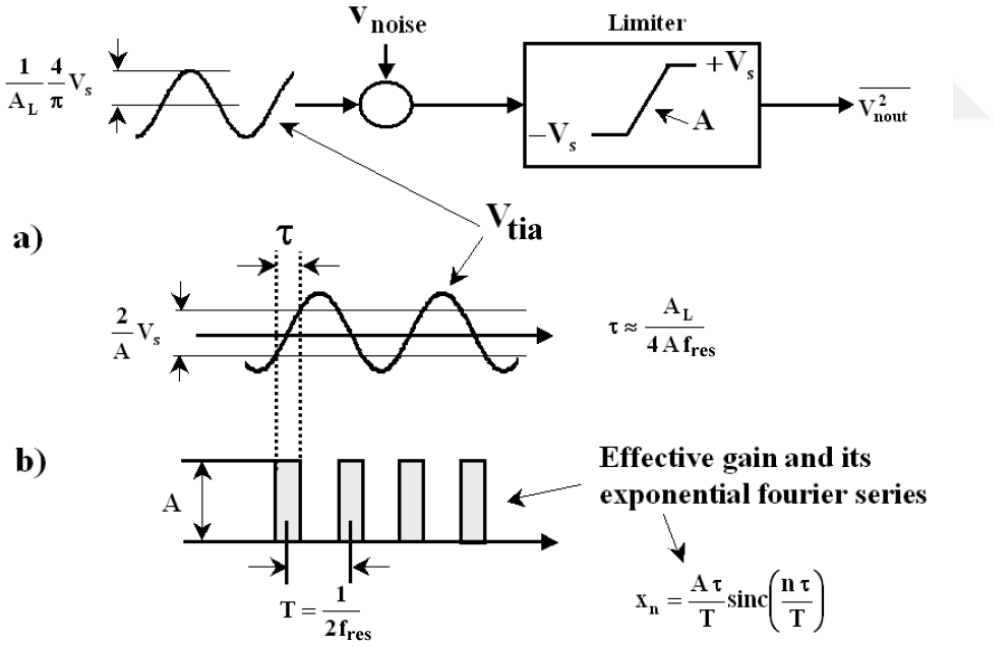


Figure 2.26: Statinoary to cyclostationary noise conversion is represented in this figure which occurs due to the nonlinear behavior of the limiter [3].

CHAPTER 3

IMPLEMENTING CLOSED-LOOP CIRCUIT IN CMOS TECHNOLOGY

3.1 Goal of the CMOS Based Design

Before starting to implement closed-loop circuit, minimum achievable far-from-carrier and close-to-carrier noise components need to be determined and estimated. Then according to these minimum values, components will be designed in CMOS Technology.

To start, the motional resistance of the resonator is assumed to determine the noise floor of the oscillator at the output at the steady state. This assumption is made because of the fact that the sustaining amplifiers provide a gain equal to the motional resistance of the resonator at the steady state. As will be shown later in this chapter, motional resistance for the DETF resonator is calculated to be about 512 kΩ. This much resistance has 4KTR$_m$=8.48$\times 10^{-15}$ V^2/Hz noise PSD. If this value is considered to be the minimum achievable noise, the far-from-carrier noise component for a driving signal of 22 mV RMS is obtained to be -107.6 dBc/Hz. 22 mV is the maximum driving signal for the resonator to operate in linear regime. This voltage will be achieved for the resonator later in this chapter as well. As a result, -107.6 dBc/Hz is assumed to be the minimum achievable far-from-carrier phase noise component at the beginning.

This is how Cadence calculates Phase noise: "Spectre RF simulation computes the total noise of the circuit, both amplitude and phase noise. What the analog circuit

design environment plots as phase noise is really the total noise scaled by the power in the fundamental oscillation mode. Close enough to the fundamental frequency, the noise is all phase noise, so what the analog circuit design environment plots of phase noise is really the phase noise as long as it is a good ways above the noise floor. Some discussions of oscillator noise based on a simple resonator/amplifier description describe the total noise, at small frequency offsets from the fundamental, as being half amplitude noise and half phase noise. In reality, for physical oscillators, near the fundamental nearly all the noise is phase noise. Therefore, these simple models overestimate the total noise by 3 dB." [46] This way of measurement is in consistent with how Wojciechowski calculates phase noise [3].

The corner frequency of the implemented sustaining circuitry with 22 mV-RMS output signal is measured in Cadence to be a few kHz which is a larger value compared to the Leeson frequency, $f_L = f_{res}/2Q = 174818/46000 = 3.8\ Hz$ (for the designed DETF MEMS resonator [4]). Hence, as represented in Figure 2.23, the output phase noise, $\phi(f)$, will show f^0, f^{-1} and f^{-3} noise components in its spectrum. f^{-3} portion is also highly dependent on Leeson frequency.

To sum up, the resonator is fabricated already, therefore there is no control on Leeson frequency, $f_{res}/2Q$. If the flicker noise has a lower PSD, then both f^{-1} and f^{-3} components will have smaller coefficients as well. Flicker noise reduction in the closed-loop implementation is limited mostly by the variable gain amplifier (not the operational amplifier) as will be shown in the next sections. Flicker noise reduction by increasing area of transistors could not completely be achieved in variable gain amplifier since by increasing the area of transistors, 3dB bandwidth gets limited and some issue regarding stability of the common mode feedback (CMFB) arises. These issues can be considered as the future works. However, the difficulty that VGA with large flicker noise PSD brings about is that, for better SNR purposes, employing two or three stages of VGA in the loop is not possible. It has been shown in [6] that the flicker noise of cascaded stages will add up before appearing at the output. This is not desirable because the flicker noise of the VGA implemented in this study is high. Therefore, a single stage VGA is used in the loop in order to keep flicker noise level as small as possible. It is also not possible to achieve a larger gain range with a single stage VGA and consequently obtaining a better SNR for the thermal noise is limited.

Better SNR is possible when the trans-impedance gain is chosen to be larger than the motional resistance of the resonator and the thermal noise contribution of the VGA is much smaller than the noise contribution of the TIA.

At the output, the flicker noise is determined by the VGA, however thermal noise is mostly due to the thermal noise contribution of the trans-impedance amplifier (thermal noise contribution of the VGA is small). The other issue is related to the thermal noise contribution of the TIA. When the resonant frequency, motional resistance and the input parasitic capacitance are large, operational amplifier with larger gain bandwidth product is necessary to be employed as the core of trans-impedance block. Large input parasitic capacitance along with a large feedback resistor will reduce input pole of the TIA to a lower frequency. This implies that, as shown in section 2.2.3, the input referred voltage noise of the operational amplifier determines the noise PSD at the output of the TIA because of the larger noise gain.

As a result, if in the future works, flicker noise contribution of the VGA can be reduced, it is possible to use cascaded stages of VGA amplifier to achieve a larger gain range. By doing this, trans-impedance gain can be increased in order to increase the SNR and obtain better far-from-carrier and close-to-carrier phase noise components.

3.2 Equivalent Electrical Model of the DETF Resonator

Equivalent electrical elements can be derived by using either equations from section 2.1.4 or by measuring resonance characteristics (Q, ω_{res} and peak value) on a Network Analyzer and building up the series RLC circuit. Obtained elements by the first method are shown in Table 3.1. Since there is a big gap between what is measured by the Network Analyzer and what is calculated in Table 3.1, it has been concluded that the resonator is under stress. The structure (DETF) inside the package is under stress that's the reason why gathered data such as motional resistance shows smaller value in Table 3.1. Thus, the collected data by Network Analyzer is used to determine the equivalent electrical model due to the fact that it represents the real behavior of the resonator.

Table 3.1: The equivalent electrical elements of the DETF resonator.

Useful Terms

Young's modulus of silicon (**E**)	$\mathbf{169\times10^{9}}$ **Pa**
Mass density of silicon ($\boldsymbol{\rho}$)	**2330 Kg/m^3**
Permittivity of vacuum ($\boldsymbol{\varepsilon_0}$)	$\mathbf{8.854\times10^{-12}}$ **F/m**

Dimensions

Length of the tine ($\boldsymbol{L_{tine}}$)	$\mathbf{500\times10^{-6}}$ **m**
Length of the capacitor plate ($\boldsymbol{L_{cap}}$)	$\mathbf{320\times10^{-6}}$ **m**
Length of the connector ($\boldsymbol{L_c}$)	$\mathbf{120\times10^{-6}}$ **m**
Width for all (**W**)	$\mathbf{10\times10^{-6}}$ **m**
Thickness of silicon layer (**h**)	$\mathbf{35\times10^{-6}}$ **m**
Capacitive gap (**g**)	$\mathbf{2\times10^{-6}}$ **m**

Calculated Mass, Stiffness, Resonance frequency and Transduction area

Transduction Area for one side, **A**	$\mathbf{1.12\times 10^{-8}}$ **m^2**
Mass, **M** = $\mathbf{0.375M_{static}+M_{dynamic}}$ = $\boldsymbol{\rho}$**hg(0.375**$\boldsymbol{L_{tine}}$**+**$\boldsymbol{L_{cap}}$ **+** $\boldsymbol{L_c}$**)**	$\mathbf{0.51\times10^{-9}}$ **Kg**
Stiffness, **k** = **(192EW^{3}h)/12**$\boldsymbol{L_{tine}^3}$	**757.12 N/m**
Resonance frequency, **f = sqrt(Stiffness/Mass)**	**193.87 kHz**

Equivalent electrical elements for DETF resonator

Coupling factor, $\boldsymbol{\eta = V_p}$ **(dC/dx)** = **40×** $\boldsymbol{\varepsilon_0 A/g^2}$	$\mathbf{99.12\times10^{-8}}$ **(F/m)**
$\boldsymbol{C_0}$**= 2(**$\boldsymbol{\varepsilon_0 A/g}$**)**	**99.12 fF**
Motional Capacitance, $\boldsymbol{C_m}$ = 2$\boldsymbol{\eta^2}$/**k**	**2.59 fF**
Motional Inductance, $\boldsymbol{L_m = M/2\eta^2}$	**259.7 H**
Motional Resistance, $\boldsymbol{R_m}$ = $\boldsymbol{sqrt(Mk)/2Q\eta^2}$	**13.9 kΩ**

3.2.1 Obtaining Equivalent Electrical Model of the Resonator by Using a Network Analyzer

Figures 3.1 and 3.2 represent the resonance test in a wider spectrum and shorter frequency range respectively. The figures show the transmission gain of the DETF resonator along with a $1M\Omega$ trans-impedance amplifier.

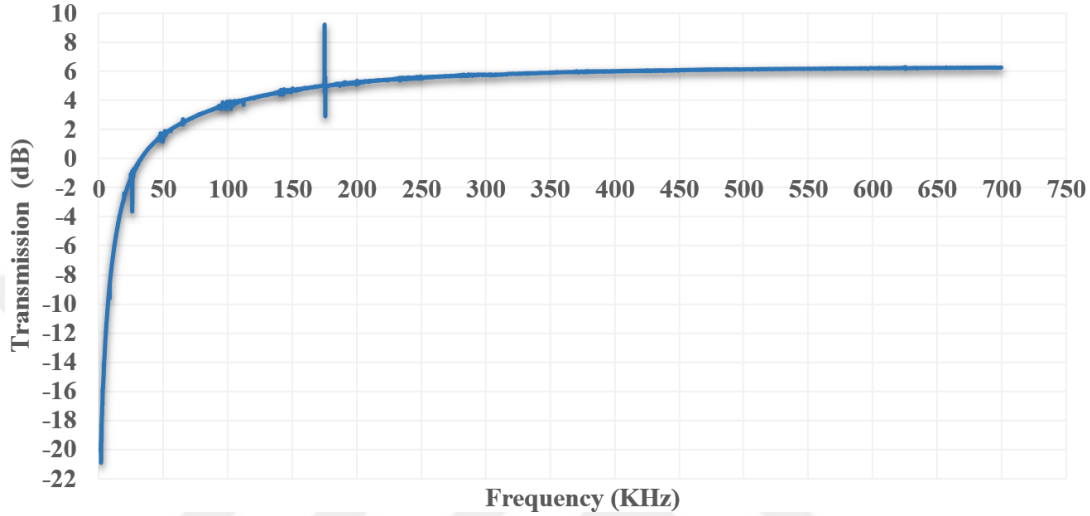


Figure 3.1: Resonance test in a wider spectrum is shown in this figure.

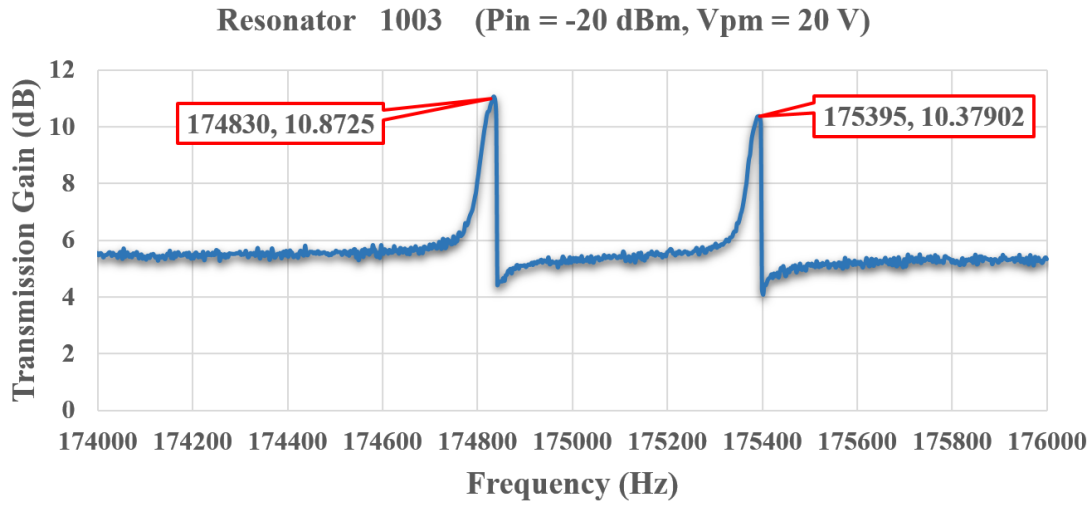


Figure 3.2: Resonance test is represented in a shorter frequency range.

The tests are accomplished by Agilent 4395A Network Analyzer while input power and proof mass DC voltage are set to -20 dBm and 20 V respectively. -20 dBm is considered to be the maximum input power when the proof mass voltage is about 20 V. Any power beyond -20 dBm brings about A-f effect [26] and nonlinear operation

of the resonator. The reference voltage on the reference port, R, is 22.36 mV. The output voltage of the trans-impedance amplifier is sensed by an active probe (Gain 1:1) on port B.

3.2.2 Quality Factor and Feedthrough Capacitance Calculations

The resonator gets nonlinear with -20 dBm (22.36 mV-RMS) input power due to high feedthrough current and spring hardening effect. In order to evaluate the feedthrough effect and obtain the approximate quality factor of the resonator, resonance test is done on the first mode of vibration with two different proof mass voltages: 20 V (Figure 3.3) and 0 V (Figure 3.4). The input power is set to -30 dBm to reduce spring hardening effect and as a result to make it possible to estimate quality factor better.

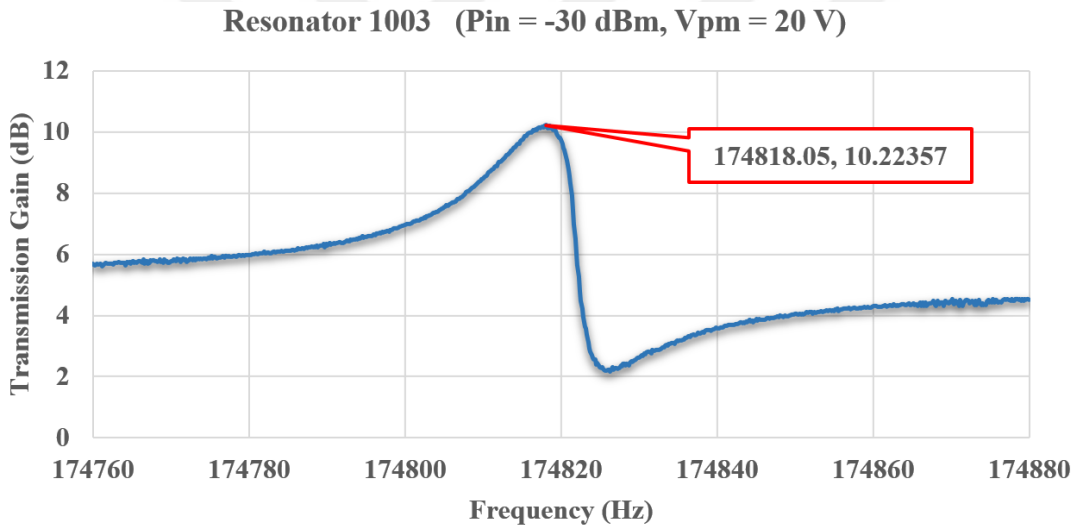


Figure 3.3: Obtained transmission gain when the proof mass voltage and input power are set to 20 V and -30 dBm.

The feedthrough capacitance is calculated by using transmission gain when the proof mass voltage is set to zero as shown in Equation 3.1.

$$\begin{aligned} TG\big(V_{PM}=0V\big)=5.05\,dB &= 20log\Big(\big|\frac{V_o}{V_i}\big|\Big) \\ &= 20log\big(2\pi f_{res}C_{ft}R_f\big) \\ &= 20log\big(2\pi\times 174818\times C_{ft}\times 1M\Omega\big) \end{aligned} \tag{3.1}$$

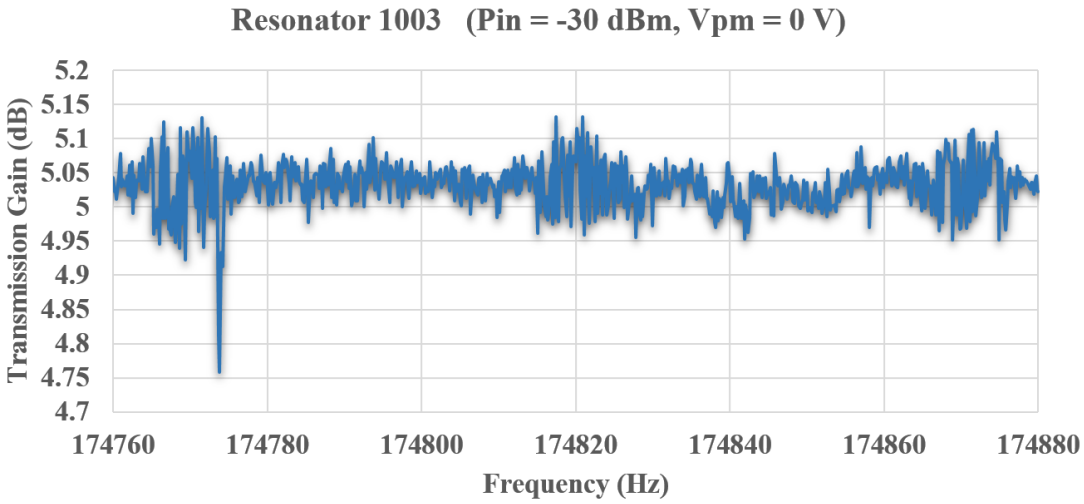


Figure 3.4: Obtained transmission gain when the proof mass voltage and input power are set to 0 V and -30 dBm.floyd

C_{ft} is obtained to be $1.74\ pF$. To calculate the quality factor of the resonator, the feedthrough current is subtracted from the first resonance mode, the following figure (3.5) is obtained

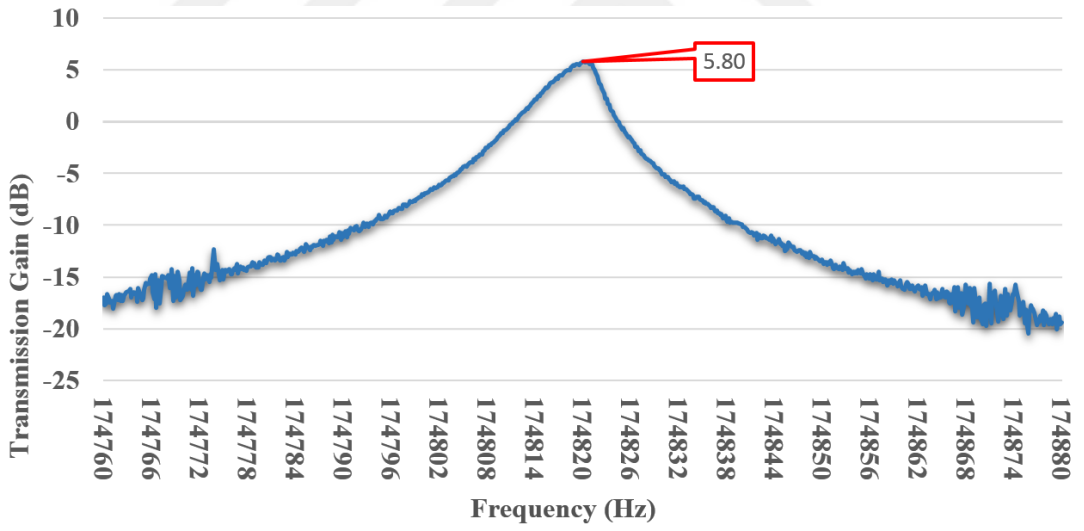


Figure 3.5: Obtained resonance after the subtraction of feedthrough current from the first mode of vibration.

Thus, the quality factor is determined by

$$\begin{aligned} Q &= \frac{f_{res}}{\Delta f} \\ &= \frac{174820}{(174822.55 - 174814.9)} = 22852 \end{aligned} \tag{3.2}$$

The peak value of the first mode of vibration is around $5.8\ dB$ as represented in Figure 3.5. The quality factor is calculated to be 22852 in Equation 3.2 and the resonant frequency is also represented in Figure 3.2 which is about 174.820 kHz. The motional resistance, capacitance and inductance of the resonator can be calculated by Equations 3.3, 3.4 and 3.5.

$$\begin{aligned} TG\big(V_{PM} = 20V\big) = 5.8\ dB &= 20log\Big(|\frac{V_o}{V_i}|\Big) \\ &= 20log\big(\frac{R_f}{R_m}\big) \\ &= 20log\big(\frac{1M\Omega}{R_m}\big) \end{aligned} \tag{3.3}$$

R_m is calculated as $511.536\ K\Omega$. C_m is obtained by using Equation 3.2.

$$\begin{aligned} Q = 22852 &= \frac{1}{R_m C_m \omega_{res}} \\ &= \frac{1}{511536 \times C_m \times 2\pi \times 174820} \end{aligned} \tag{3.4}$$

that is about $77.835\ aF$. And finally, L_m is determined by

$$\begin{aligned} \omega_{res}^2 = \big(2\pi \times 174820\big)^2 &= \frac{1}{C_m L_m} \\ &= \frac{1}{77.835 \times 10^{-18} \times L_m} \end{aligned} \tag{3.5}$$

which is obtained to be 10.648 kH. To check the accuracy of the achieved RLC model, transfer function of the RLC model along with a $1M\Omega$ TIA is written as below (Equation 3.6) and the Bode diagram is plotted in MATLAB as shown in Figure 3.6.

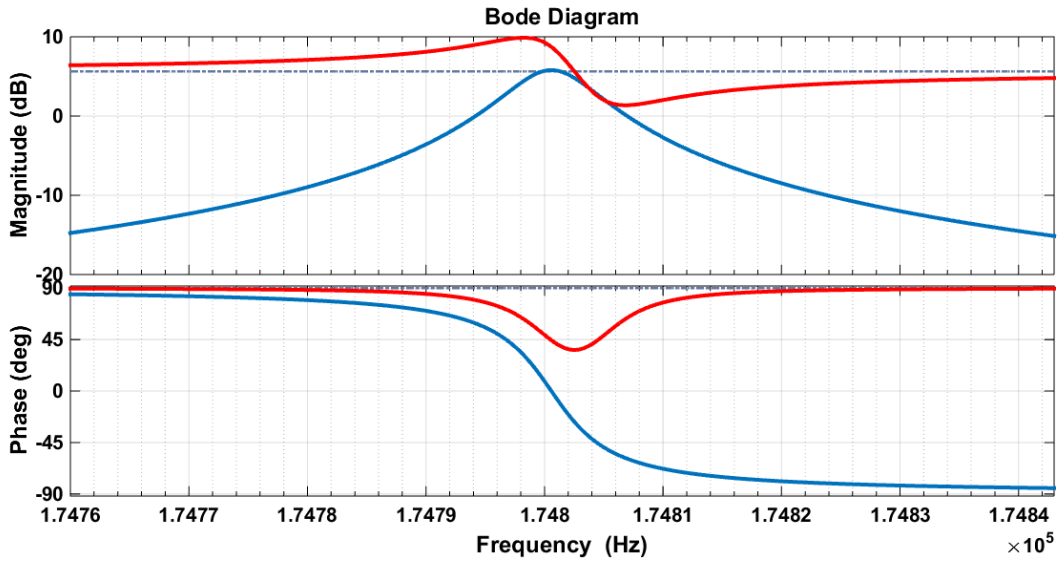


Figure 3.6: The equivalent RLC model is checked in MATLAB.

$$
\begin{aligned}
Gain\big(DETF + TIA\big) &= \frac{V_{out}}{V_{in}} \\
&= \frac{R_f C_m s}{L_m C_m s^2 + R_m C_m s + 1} + R_f C_{ft} s \\
&= \frac{\frac{R_f}{R_m}\frac{\omega_{res}}{Q} s}{s^2 + \frac{\omega_{res}}{Q} s + \omega_{res}^2} + R_f C_{ft} s \\
&= \frac{93.72\ s}{s^2 + 48.06\ s + 1.21e12} + 1.74e-6\ s
\end{aligned}
\tag{3.6}
$$

3.3 CMOS ASIC

A sine wave oscillator with an automatic gain control block has superior performance in comparison to a square wave closed-loop circuit with a limiter (Figure 2.14). Its far-from-carrier phase noise performance is better than square wave oscillator [3]. Because of this fact, the sine wave oscillator with an AGC block (Figure 3.7) is chosen to be implemented in CMOS Technology.

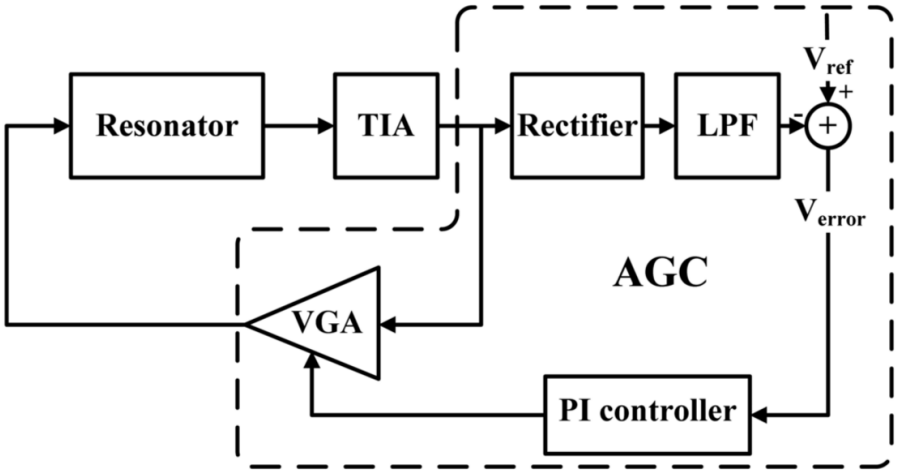


Figure 3.7: Sine wave oscillator along with an AGC block [47].

As shown in Figure 3.7, there are two main loops in the topology. Oscillator loop which produces the oscillation and AGC loop which stabilizes the oscillation amplitude. First loop to implement is the oscillator. It consists of a TIA and a VGA in its feedforward path and the DETF resonator in its feedback.

3.3.1 Trans-impedance Amplifier (TIA)

Trans-impedance amplifier is the first block which is responsible for the current to voltage conversion with minimum added noise. One of the important parameters that determines the performance of the TIA amplifier is the input parasitic capacitance. Larger input capacitance not only increases the noise gain (NG) as shown in section 2.22 but also determines the stability of the TIA as discussed in section 2.2.1. The input pole, which is a result of a higher parasitic capacitance at the input node, will fall in the unity gain bandwidth (GBW) of the op-amp and will cause ringing or total unstability after building up the feedback loop around the operational amplifier.

Parasitic capacitance at the input node of trans-impedance amplifier is the sum of parasitic capacitances of the ESD pad on the IC and the pad on the vacuum package of the resonator which are respectively around 3 pF and 12 pF (2 pads are used to do feedthrough cancellation). Total parasitic capacitance, with a better safety margin, is taken to be around 16 pF.

3.3.1.1 Operational Amplifier

Operational amplifier (Figure 3.8) is constructed in Cadence based on the design in [48,49]. This symmetric folded cascode OTA with floating current sources and output (common source) buffer stage provides high gain and better noise performance. It takes advantage of floating current sources at the Class AB buffer stage to reduce the offset error. These floating sources equalize the voltages across M23/M24 and M27/M28. It has been shown in [48] that the current flowing out of M28 (downwards) sees $g_{m_{24}} r_{o_{24}} (r_{o_{22}} \parallel r_{o_{31}})$ resistance and does not see the floating current source on the path.

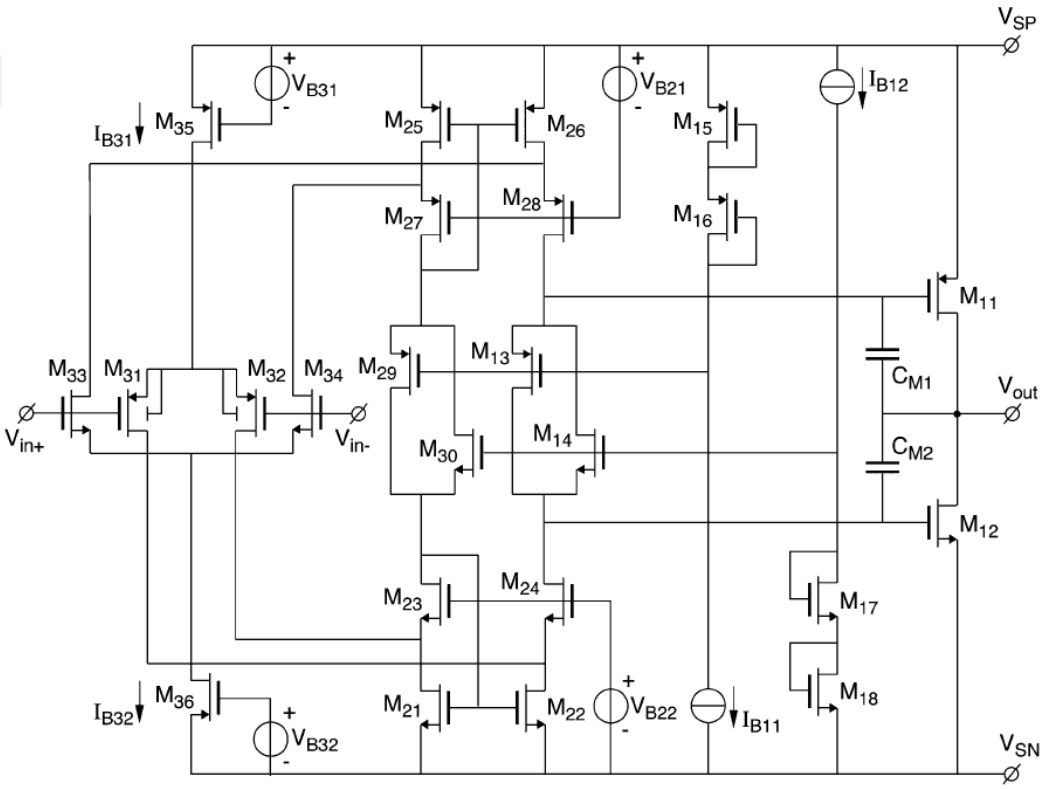


Figure 3.8: Operational amplifier [49].

Current mirror transistors are chosen to have higher areas. According to the flicker noise equation (3.8), larger transistors show smaller PSD for the flicker noise. In addition, long transistors reduce the effect of channel length modulation and error in copying current. Because of these reasons, channel length of the transistors in current mirrors is selected to be $5\ \mu m$. The trans-conductance of current mirror transistors are also chosen to have a smaller value compared to the trans-conductance of

input differential pair since input referred voltage noise is dependent on their ratio, $e_n^2 \, \alpha \, (g_m(mirror)/g_m(diff))^2$.

Signal level in the oscillator will be small (about 22 mV RMS), smaller than the input common mode range of operational amplifiers. Therefore there is no need to be worried about the input common mode range of complementary differential pairs. Using complementary differential pairs at the input stage of the folded cascode OTA helps to increase the gain bandwidth product due to the fact that the total trans-conductance is the summation of trans-conductances of two differential pairs, $g_m(nmos) + g_m(nmos)$. Differential Pair transistors do not need to be wider even though having wide differential pair reduce flicker noise. Current mirror transistors are wide. Wide differential pair decreases mirror pole considerably and consequently unity gain bandwidth drops.

Noise performance of folded cascode OTA is mostly defined by the current mirrors and the input differential pairs. g_m is defined by Equation 3.7 and it has been shown in [50] that the input referred voltage noise is proportional to the ratio of transcoductances of the input differential pairs and the current mirrors, $g_{m,mirror}/g_{m,diff}$. Input referred voltage noise of a long channel MOS transistor is also given by Equation 3.8 [51].

$$g_m = \sqrt{2I_d \mu C_{ox} \frac{W}{L}} = \frac{2I_d}{V_{GS} - V_{TH}} \tag{3.7}$$

$$\overline{V}_{n,in}^2 = 4kT\frac{2}{3}\frac{1}{g_m} + \frac{K}{C_{ox}WLf} \tag{3.8}$$

Equation 3.8 implies that larger transistors have smaller flicker noise PSD and larger trans-ductance brings about smaller thermal noise. To reduce the thermal noise of a MOSFET, trans-conductance of the transistor (Equation 3.7) needs to be increased. This is done by increasing either I_d or W/L ratio. Since r_o is proportional to I_d^{-1}, increasing I_d and W/L are made up to a point that increasing them further do not bother GBW requirements of the operational amplifier.

Output pole of the folded cascode OTA will be the dominant pole in the operational

amplifier because its output resistance is so large compared to that of the buffer stage (second stage). To have a better phase margin after compensation, it has been shown in [49] that the unity gain bandwidth is selected to be half of the second pole (buffer stage).

$$GBW = \frac{1}{2}\frac{g_{m_2}}{2\pi C_L} \tag{3.9}$$

The unity gain bandwidth of the operational amplifier is chosen to be about $10\ MHz$ which is enough for our application. In addition, according to the maximum parasitic capacitance calculated in section 3.3.1, the maximum capacitive load to be driven by the operational amplifier is determined to be $20\ pF$. By plugging GBW and C_L into Equation 3.9, trans-conductance for the second stage is achieved to be about $g_{m_2} = g_{m_{11}} + g_{m_{12}} = 2.5\ mA/V$. Therefore, $g_{m_{11}}$ and $g_{m_{12}}$ will be equal to $1.25\ mA/V$. The approximate gain for the operational amplifier is also given by

$$\begin{aligned} A_V &= G_{m_1} R_{L_1} \times G_{m_2} R_{L_1} \\ &= G_{m_1}\left\{\left(g_{m_{24}} r_{o_{24}} (r_{o_{22}} \parallel r_{o_{31}})\right) \parallel \left(g_{m_{28}} r_{o_{28}} (r_{o_{26}} \parallel r_{o_{33}})\right)\right\} \\ &\quad \times G_{m_2}\left(r_{o_{11}} \parallel r_{o_{12}}\right) \end{aligned} \tag{3.10}$$

Where G_{m_1} is the trans-conductance of the first stage (folded cascode OTA) and is equal to the summation of $g_{m_{ndiff}}$ and $g_{m_{pdiff}}$. Trans-coductance of second stage, G_{m_2}, is also the summation of two trans-coductances from transistors M11 and M12 (common source stages) and can be written as $g_{m_{11}} + g_{m_{12}}$.

To avoid channel length modulation in $0.35\ \mu m$ CMOS Technology, minimum channel length for the transistors are chosen to be $3 \times 0.35\ \mu m \approx 1\ \mu m$. To obtain a higher gain, smaller current is chosen for the folded cascode OTA. With $53\ \mu A$ current at the tail of differential pairs, maximum achievable trans-conductance for the differential

pair before entering subthreshold region is obtained to be $492.8\ \mu A/V$, which results in $G_{m_1} = 985.6\ \mu A/V$.

The implemented operational amplifier will be used in the core of the TIA amplifier and the PI controller, it will also be used as the buffer to derive capacitive loads up to $20\ pF$. To drive this much load and to avoid unstability, the operational amplifier needs to be compensated with sufficiently large compensation capacitors. The compensation capacitor, as shown in [49], is obtained roughly by

$$C_{M1} = C_L \frac{G_{m_1}}{G_{m_2}} \tag{3.11}$$

By plugging $G_{m_1} = 985.6\ \mu A/V$, $G_{m_2} = 2.5\ mA/V$ and $C_L = 20\ pF$ into Equation 3.11, C_{M1} is obtaned to be about $7.9\ pF$. Output resistance of the second stage after implementation is also obtained to be $R_{out} = (r_{o11} \| r_{o12}) = (129.2\ k\Omega \| 197.4\ k\Omega) = 78 k\Omega$. Output resistance of the folded cascode OTA is also achieved to be $13\ M\Omega$. The total gain is calculated to be about $2.5 \times 10^6\ V/V$ or $128\ dB$. Figure 3.9 represents AC response of the operational amplifier with $C_L = 20\ pF$.

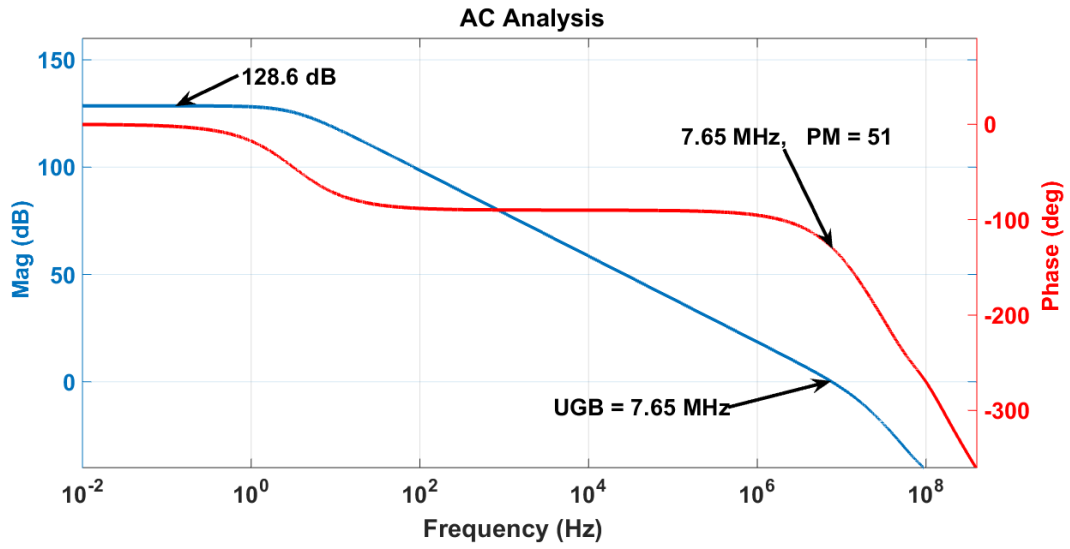


Figure 3.9: AC Analysis of the operational amplifier.

Slew rate is the maximum time rate change at the output of the operational amplifier which is obtained for the op-amp as shown in Figure 3.10. Both positive and negative slew rates, $SR\pm$, are about $4.5\ V/\mu S$. To determine the highest frequency sine wave

that will not be distorted by the slew rate (SR), the full bandwidth product (FPBW) [52] is defined in Equation 3.12. If maximum peak-to-peak voltage in the loop is chosen to be $0.4\ V$ which is much greater than $22\ m(rms)$ voltage at the output of the oscillator, the FPBW is achieved to be $3.6\ MHz$. It implies that this op-amp is able to have a sinusoidal signal with $0.4\ V(p-p)$ voltage and up to $3.6\ MHz$ frequency at the output with minimum distortion.

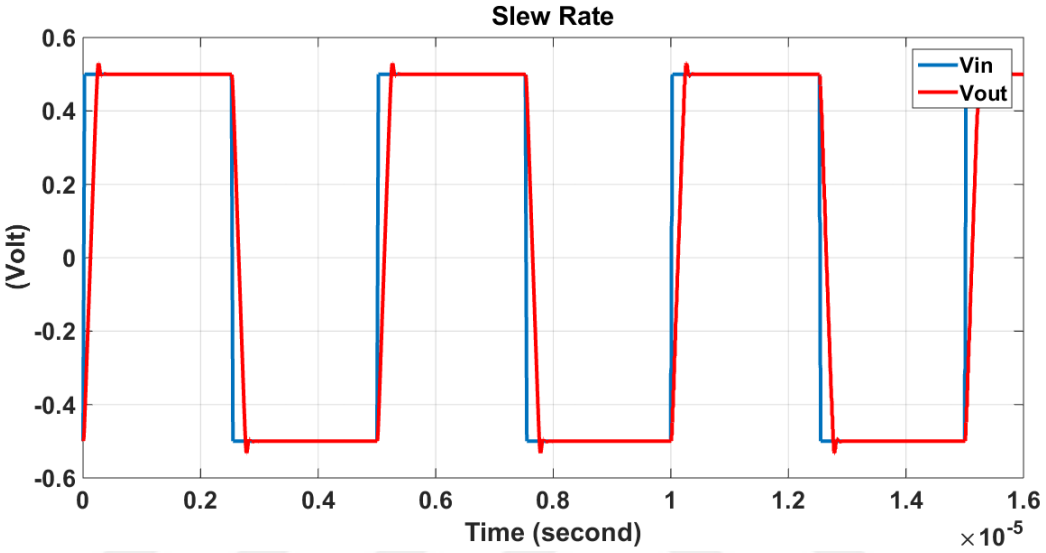


Figure 3.10: Positive and negative slew rates of the operational amplifier.

$$FPBW = \frac{SR}{\pi V_{out}(p-p)} \tag{3.12}$$

Obtained input referred voltage noise is also represented in Figure 3.11. At 174.818 kHz frequency, noise PSD is $6.85\ nV/\sqrt{Hz}$. Unity gain AC response of the op-amp is also represented in Figure 3.12. Small amount of peaking exists at higher frequencies which is due to 51 degree phase margin (PM). For higher PMs such as 60 degrees, there will be small amount of peaking in AC Analysis.

Common mode rejection ratio (CMRR) and power supply rejection ratios (PSRR$\pm$) for both supply voltages are represented in Figure 3.14.

The transistor level operational amplifier schematic is shown in Figure 3.13. The implemented layout of the operational amplifier is represented in Figure 3.15. Common Centroid layout with multi fingered gates is the technique used to draw the layout.

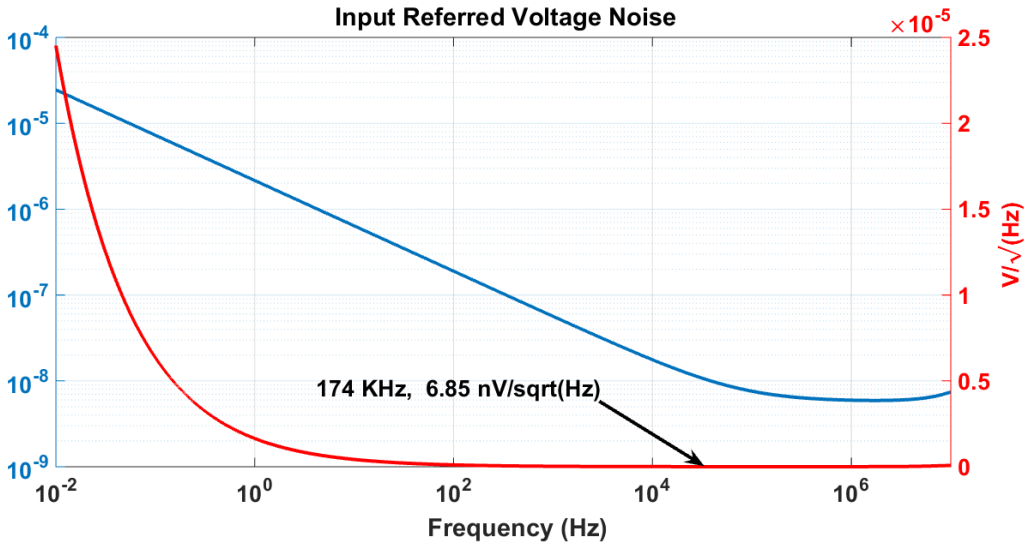


Figure 3.11: Input referred voltage noise of the operational amplifier.

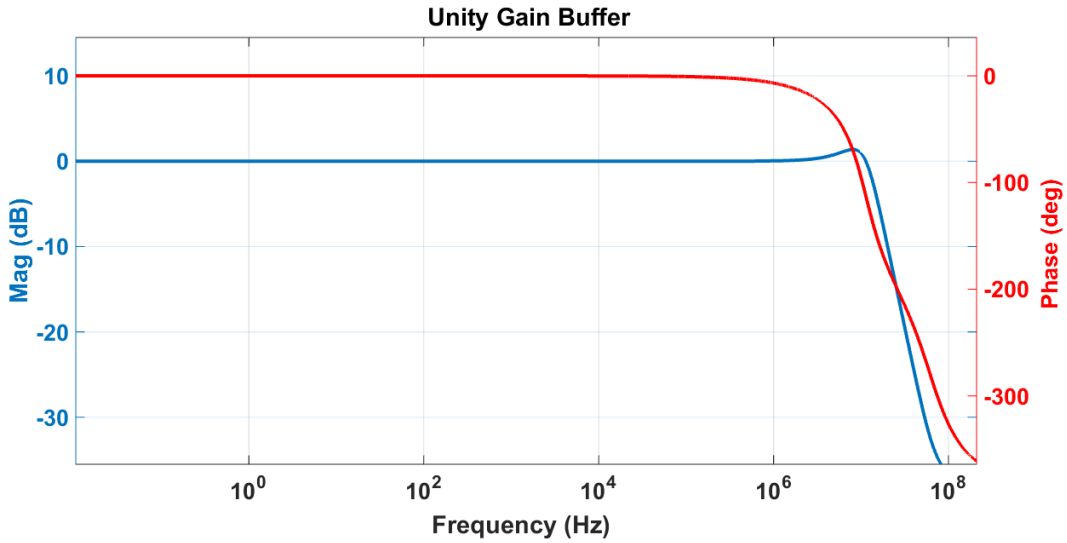


Figure 3.12: Unity gain AC response of the operational amplifier.

Cross coupling of differential pair transistors or current mirror transistors serve immune from thermal gradients and other processing related gradients. Multi-fingering saves space and reduces series resistance in gate. Dummy transistors are also used to equalize the parasitic capacitance seen by drain and source of differential pair and current mirror transistors. This way, the boundary conditions for ending transistors are the same as that of inner transistors. Thus, minimum error will exist in copying current in current mirrors and minimum mismatching and offset in the input differential pairs with common centroid layout.

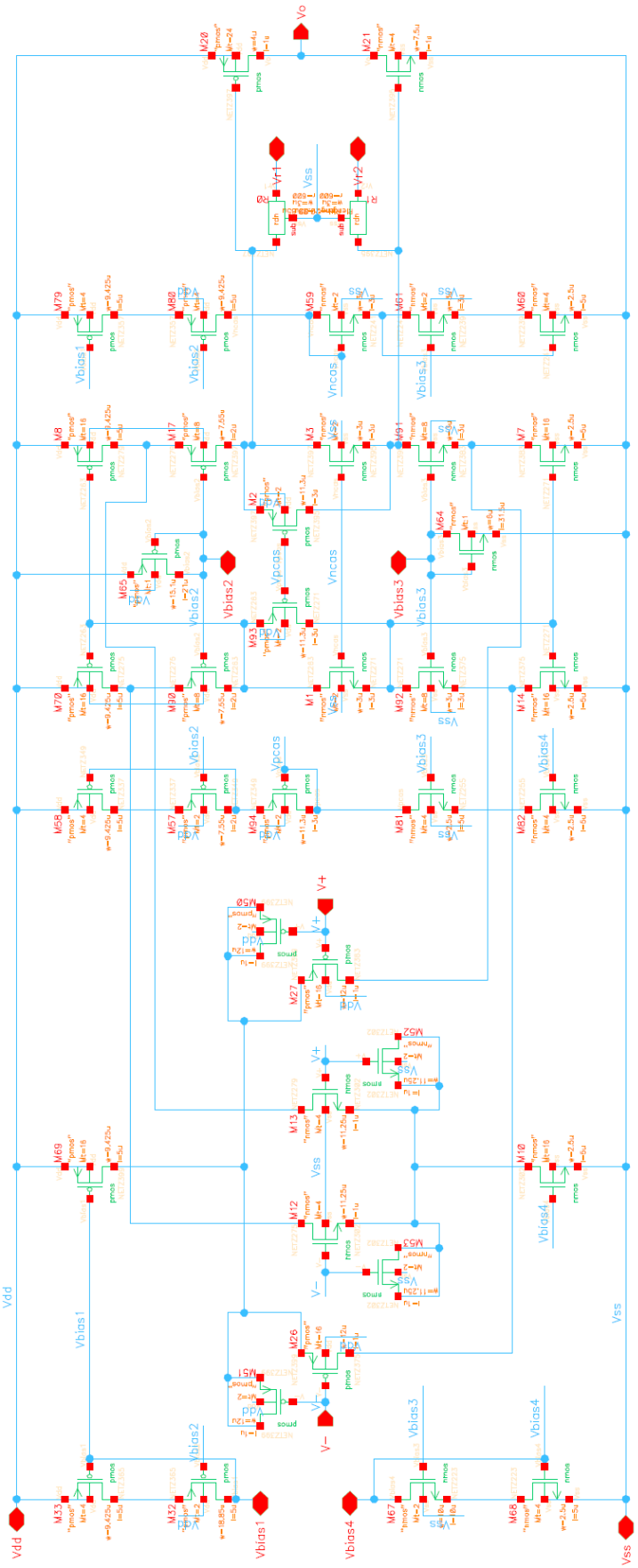


Figure 3.13: Transistor level design of the operational amplifier.

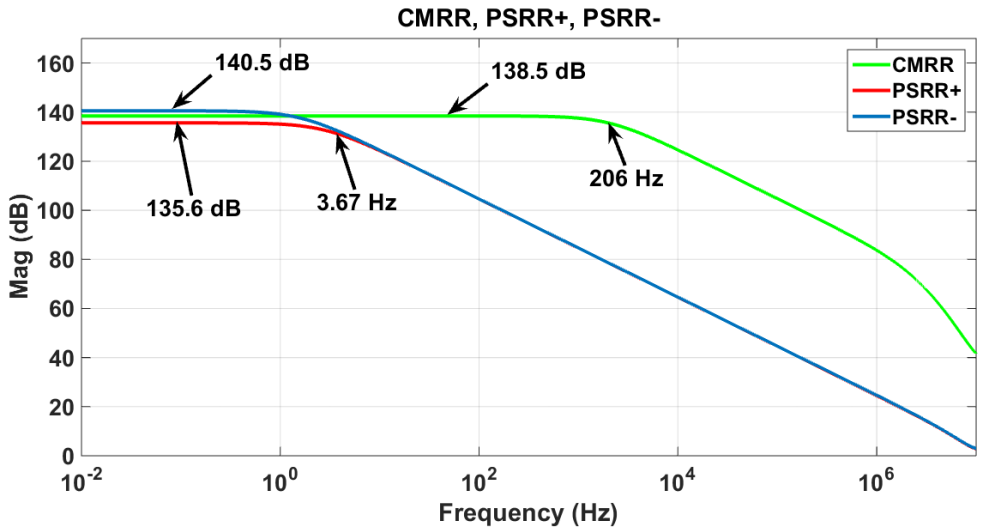


Figure 3.14: CMRR, PSRR- and PSRR+ of the implemented operational amplifier.

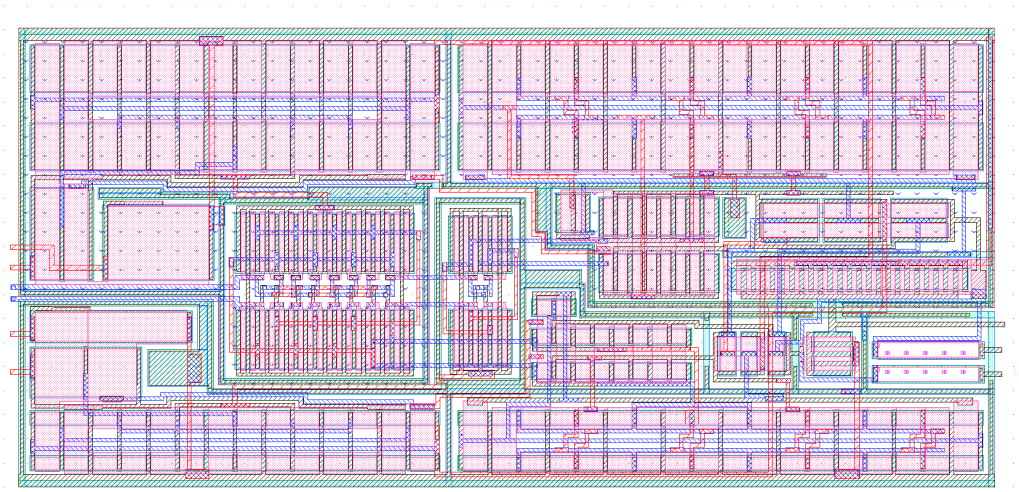


Figure 3.15: Layout of the operational amplifier.

3.3.1.2 TIA Stability and Noise Performance

Based on the current to voltage converting element (capacitor or resistor) TIAs are categorized as trans-resistance and trans-capacitance amplifiers. The implemented TIA with resisitive feedback, $R_f \| 1/(C_f s) \approx R_f$, is shown in Figure 3.16. The TIA with capacitive feedback, $R_f \| 1/(C_f s) \approx 1/(C_f s)$, is represented in Figure 3.18 as well. A differentiator is added in series with capacitive TIA to compensate 90 degree additional phase shift made by the feedback capacitor. One of the main advantages that the trans-capacitance amplifiers have over trans-resistance ones is that the trans-capacitance amplifiers are considered to be overcompensated (over-damped) second

order systems when the feedback pole is much smaller that the GBW of the op-amp. They are much immune from high input parasitic capacitance. On the other hand, trans-resistance amplifiers need to be compensated. Proper feedback capacitor is chosen to introduce a zero in the transfer function of trans-resistance amplifier to compensate the phase shift that the input pole (input parasitic capacitance) causes in its feedback loop. AC analysis and output referred voltage noise of the implemented trans-capacitance amplifier are shown in Figures 3.18 and 3.19 respectively. AC analysis and output referred voltage noise of the compensated trans-resistance amplifier are also represented in Figures 3.21 and 3.20 respectively.

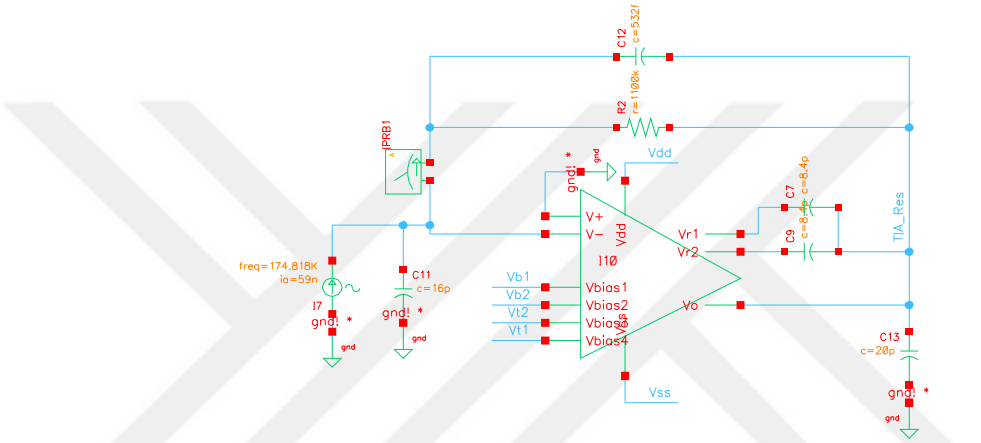


Figure 3.16: TIA with resisitive feedback (Trans-resistance).

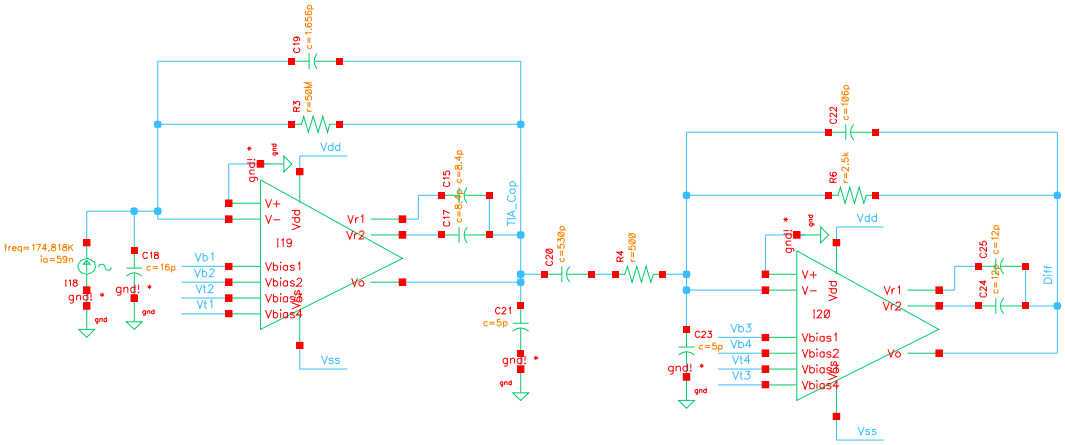


Figure 3.17: TIA with capacitive feedback (Trans-capacitance).

To have a full range operation - maximum gain at start-up and unity gain at steady state - gain of the TIA block is chosen with respect to the gain of the VGA. Trans-impedance gain is selected to be 735 $k\Omega$ (high pass filter and feedback capacitor are

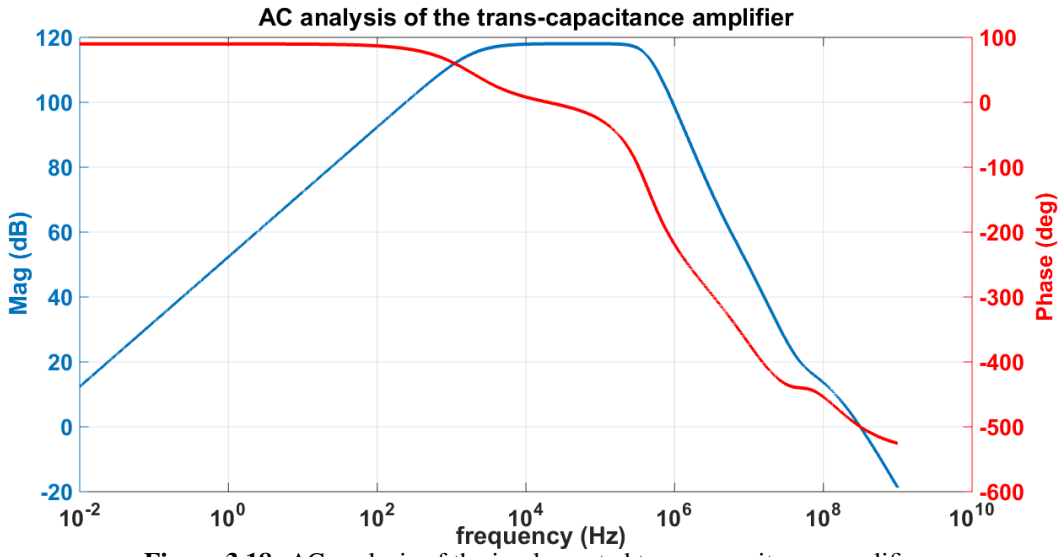


Figure 3.18: AC analysis of the implemented trans-capacitance amplifier.

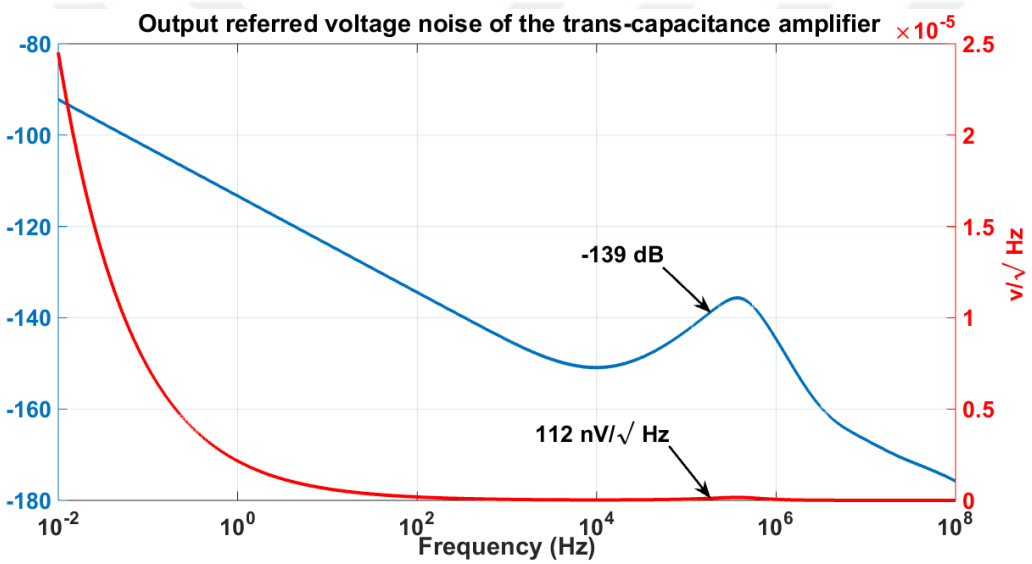


Figure 3.19: Output referred voltage noise of the implemented trans-capacitance amplifier.

taken into account). The feedback resistor for quality factor of one is chosen to be $1.1\ M\Omega$, C_f is also achieved to be $532\ fF$ as shown in section 2.2.3. Now with the above mentioned parameters, output referred rms noise and 3dB bandwidth can be calculated. Quality factor of the TIA amplifier is one, obtained unity gain bandwidth of the operational amplifier is $7.65\ MHz$ and the input parasitic capacitance is also equal to $16\ pF$. Thus the output rms noise voltage of the trans-resistance amplifier will be achieved by Equation 2.22 to be around $150\ \mu V$. Input and output poles and $3dB$ cut-off frequency of the trans-resistance amplifier are shown in Figure 3.21. Phase error for the TIA amplifier at $174.818\ kHz$ frequency is about 60 degrees. Due to Q=1, there will be a little peaking in the AC response of the TIA.

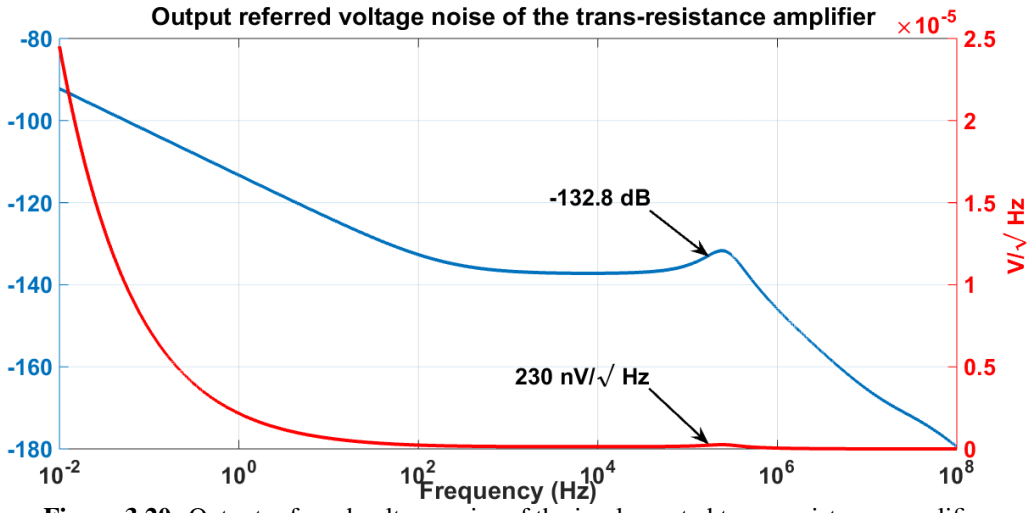


Figure 3.20: Output referred voltage noise of the implemented trans-resistance amplifier.

The loop is constructed by both the trans-capacitance amplifier along with the differentiator and the trans-resistance amplifier. However, since the gain of trans-capacitance amplifier is larger than that of the trans-resistance amplifier, at the steady state they provide the same noise floor for the phase noise. To save some space, trans-resistance amplifier is employed in the closed loop circuit implementation in CMOS technology. The specifications of the constructed operational and trans-resistance amplifiers are represented in Tables 3.2 and 3.3.

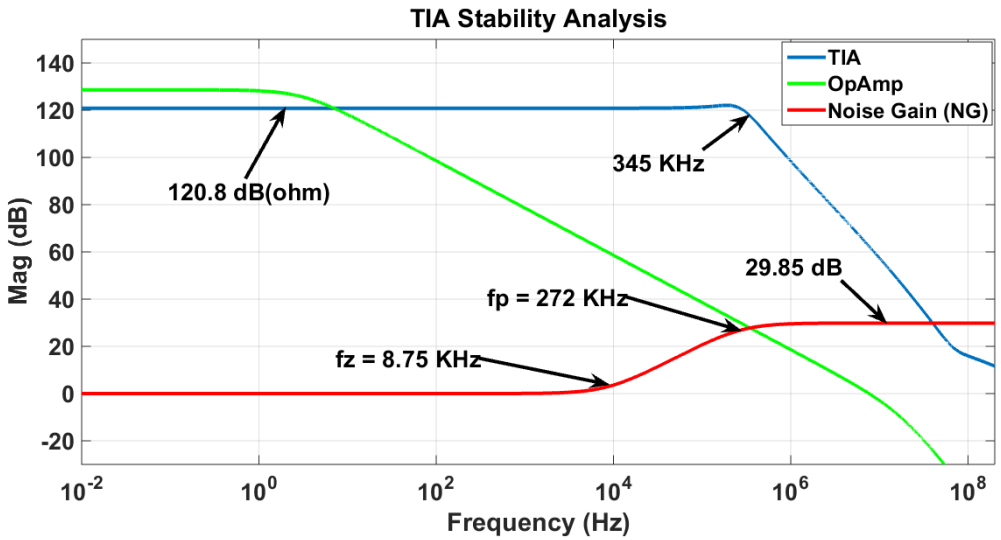


Figure 3.21: AC analysis of the compensated trans-resistance amplifier.

Table 3.2: The specifications of the operational amplifier.

Gain	128.6 dB (2.69×10^6 V/V)	**Phase Margin**	51°
Area	95.4 µm×202.9 µm	**Power Dissipation**	600 µA
GBW	7.65 MHz	**Power Supply**	±1.65
SR±	4.5 V/µs	**CMRR**	135.5 dB
Output Resistance	78 kΩ	**Input Referred Voltage Noise**	6.85 nV/$\sqrt{\text{Hz}}$ at 174 kHz

Table 3.3: The specifications of the trans-resistance amplifier.

Gain	120.8 dBΩ (1.096 MΩ)	**BW**	345 kHz
Quality Factor	1	**Output Noise**	150 µV (rms)
C_f	532 fF	**R_f**	1.1 MΩ
C_P	16 pF	**Output Referred Voltage Noise**	230 nV/$\sqrt{\text{Hz}}$ at 174 kHz

3.3.2 Biasing Circuit

PVT (Process, Voltage and Temperature) insensitive reference current from [48] is used in this thesis. The core of this biasing block is XFAB's reference current with a modification in the resistor to obtain 6.1 μA nominal current. Figure 3.22 represents the current change with respect to temperature. The temperature coefficient of the output current is obtained to be -1177 ppm/°C. The implemented layout of the current reference is represented in Figure 3.23.

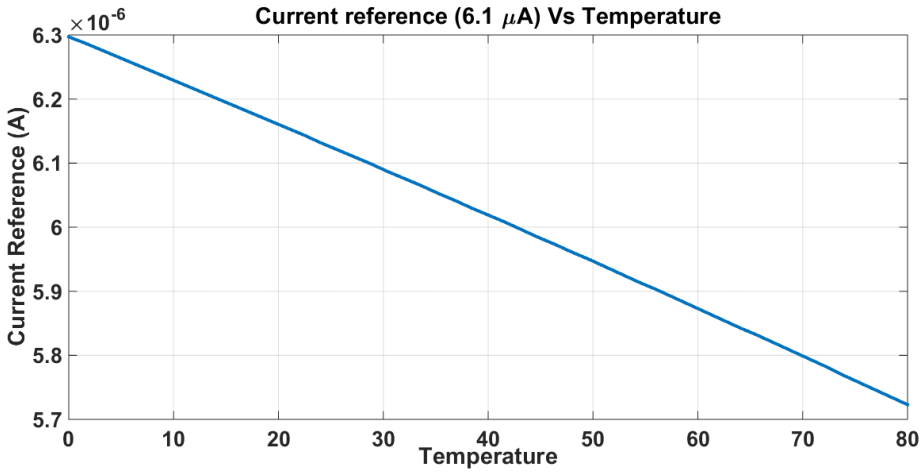


Figure 3.22: Current reference with respect to temperature is represented in this figure.

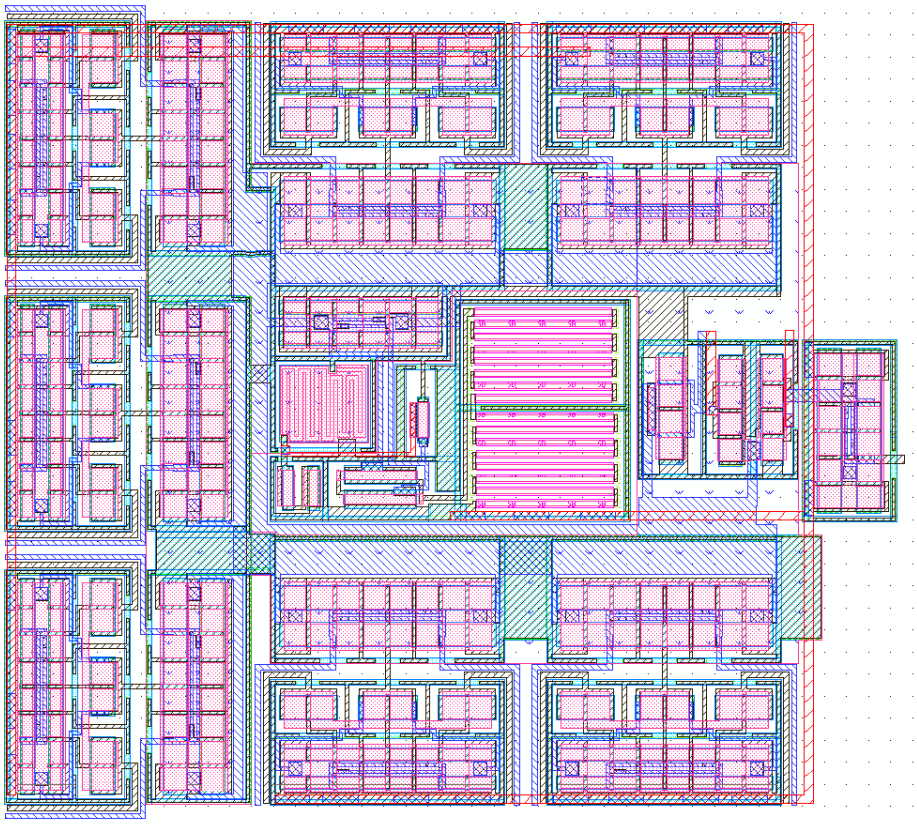


Figure 3.23: The layout of the implemented current reference.

3.3.3 Automatic Gain Control Loop (AGC)

The core of an automatic gain control block is a VGA (variable gain amplifier) as shown in Figure 3.7. In general, an AGC loop automatically controls the gain of variable gain amplifier in response to the changing input. By doing this, AGC can maintain a constant amplitude at the output. In telecommunication applications, VGA should have linear-in-dB gain profile to obtain a constant and signal independent settling time. In other words, obtaining constant settling time requires that the AGC circuit is exponentially controlled [53].

In the AGC loop (Figure 3.7), the output voltage of the VGA is peak detected and compared to a reference voltage (set point), V_{sp}, by an error detector. Then, the output of the error amplifier will be applied to a PI controller to adjust the gain of the variable gain amplifier. This feedback system is able to adjust gain according to the input voltage.

3.3.3.1 Linear-in-dB Variable Gain Amplifier (VGA)

The gain controlling mechanism in this type of VGA is in the form of approximated (pseudo) exponential function. An exponential control voltage is required to obtain linear-in-dB gain. CMOS transistors operating in subthreshold region, have exponential characteristics. However it is not common to use CMOS transistors in subthreshold because of their poor noise and bandwidth performances. Thus, pseudo exponential function generator (Figure 3.24) or parasitic bipolar transistors are widely used to overcome this problem in CMOS technology.

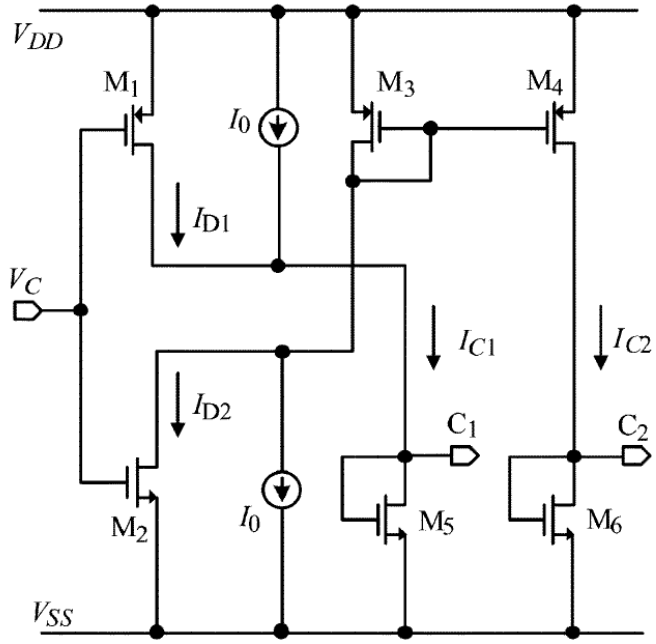


Figure 3.24: Circuit schematic of the control stage in the linear-in-dB variable gain amplifier [53].

Typically gain is controlled by the output impedance in many VGA circuits. The dominant pole usually comes from the output node as well. Thus, it can be concluded that the bandwidth is changing by the control voltage. The main drawback of the bandwidth being inversely proportional to gain, is the noise variation in high and low gains. The approximate gain of VGA (Figure 3.25) is determined by

$$A_{vga} = \frac{g_m(input)}{g_m(load)} \tag{3.13}$$

$$
\begin{aligned}
A_{vga} &= \sqrt{\frac{(\frac{W}{L})_{input} \times I_{C2}}{(\frac{W}{L})_{load} \times I_{C1}}} \\
&= \sqrt{\frac{(\frac{W}{L})_{20}}{(\frac{W}{L})_{19}} \times \frac{K + (1 + aV_c)^2}{K + (1 - aV_c)^2}}
\end{aligned}
\tag{3.14}
$$

where a is equal to V_{ov}^{-1} (the over drive voltage of the MOSFET transistor) and K is equal to $(a^2 I_0)/K_p$. K_p is the trans-conductance parameter of a PMOS transistor and is equal to $\mu_p\ C_{ox}$. Equation 3.13 is an approximation of the actual gain because it has been considered that $K_p \approx K_n$ and $V_{ov}(NMOS) \approx V_{ov}(PMOS)$.

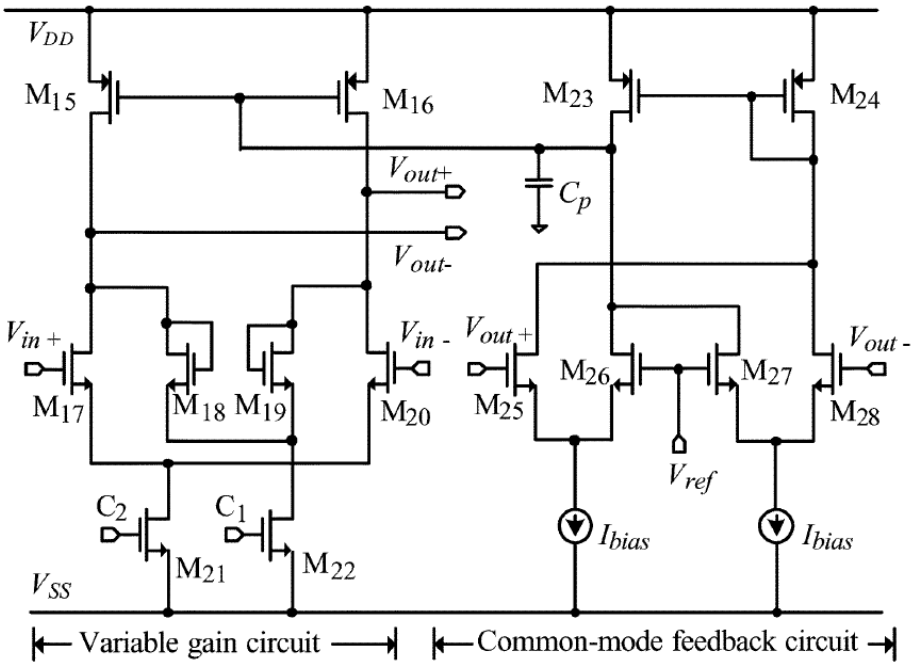


Figure 3.25: Circuit schematic of the amplifying stage in the linear-in-dB VGA [53].

To avoid any unstability, the gain of the common mode feedback loop (Figure 3.25) is chosen to be a smaller value. It is about $18\ dB$ or equivalently $7.94\ V/V$. In addition to smaller gain, a big capacitor is added to the output node of the error amplifier to reduce its bandwidth. The obtained gain for the variable gain amplifier is shown in Figure 3.26. The gain can be approximated and determined by Equation 3.15.

$$A_{VGA}(dB) \;=\; 18(\frac{dB}{V})V_c + 8.8(dB) \tag{3.15}$$

or equivalently might be rewritten as

$$\begin{aligned} A_{VGA} &= 2.75 \times 10^{0.9V_c} \\ &= 2.75 \times e^{2.3\times 0.9V_c} = 2.75 \times e^{2.07V_c} \end{aligned} \tag{3.16}$$

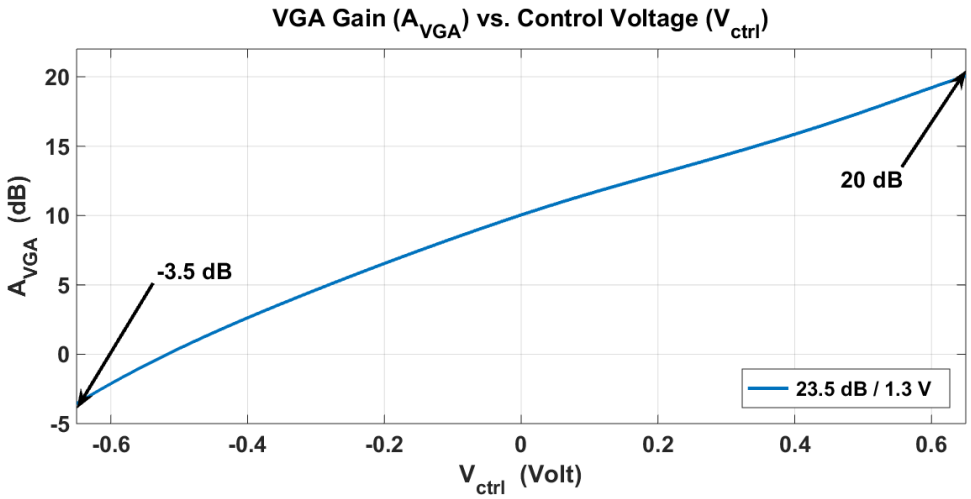


Figure 3.26: VGA gain versus control voltage.

As shown in [53], the output noise of the VGA can be reduced by decreasing the trans-conductance of diode connected loads and current mirrors. Output referred voltage noise at 174.818 kHz frequency with respect to control voltage is represented in Figure 3.27. Thermal noise contribution of the VGA to the overall open-loop noise is small in comparison to that of trans-resistance amplifier (section 3.3.1.2). The thermal noise contribution of the VGA is small for the whole range of control voltage. On the contrary, its flicker noise contribution is too large in comparison to that of trans-resistance amplifier as represented in Figures 3.28 and 3.20.

The transistor level circuit schematic and the implemented layout of the variable gain amplifier are represented in Figures 3.29 and 3.30 respectively.

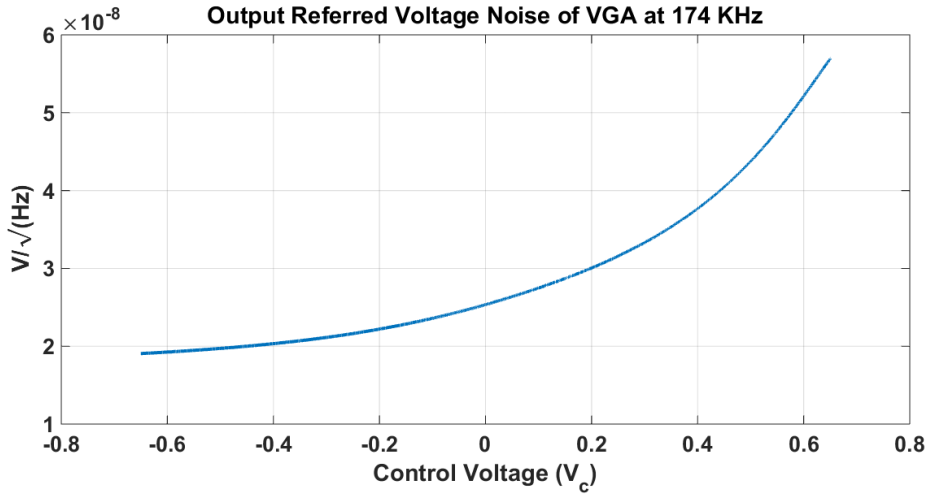


Figure 3.27: Output referred voltage noise of the VGA at 174KHz.

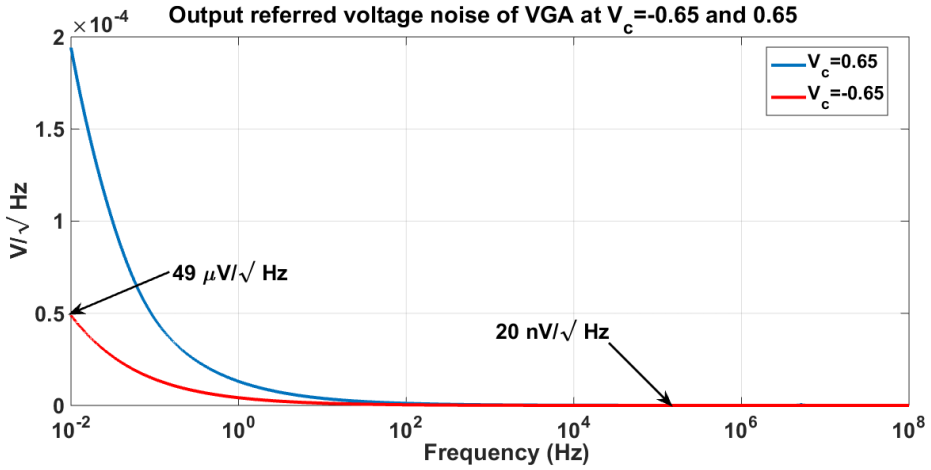


Figure 3.28: Flicker noise of the VGA has higher contribution to the output flicker noise.

3.3.3.2 Amplitude Detector and Error Amplifier (Instrumentation Amplifier with Gain = 1)

Signal level in the loop is small (about 22 mV-RMS). To rectify this small signal and then detect its amplitude after passing through a low pass filter, a super diode is required (Figure 3.31). The advantage of employing a super diode is that the on voltage of diode or MOSFET gets divided by the gain of the op-amp. The configuration in [52] is used for peak detection. The only important requirement that needs to be satisfied to have less distorted rectified signal is to use an operational amplifier with a unity gain bandwidth ten times greater than the resonant frequency. This guarantees when the super diode is switching from off to on mode, the output signal gets less distorted by the slew rate of the op-amp (Figure 3.32).

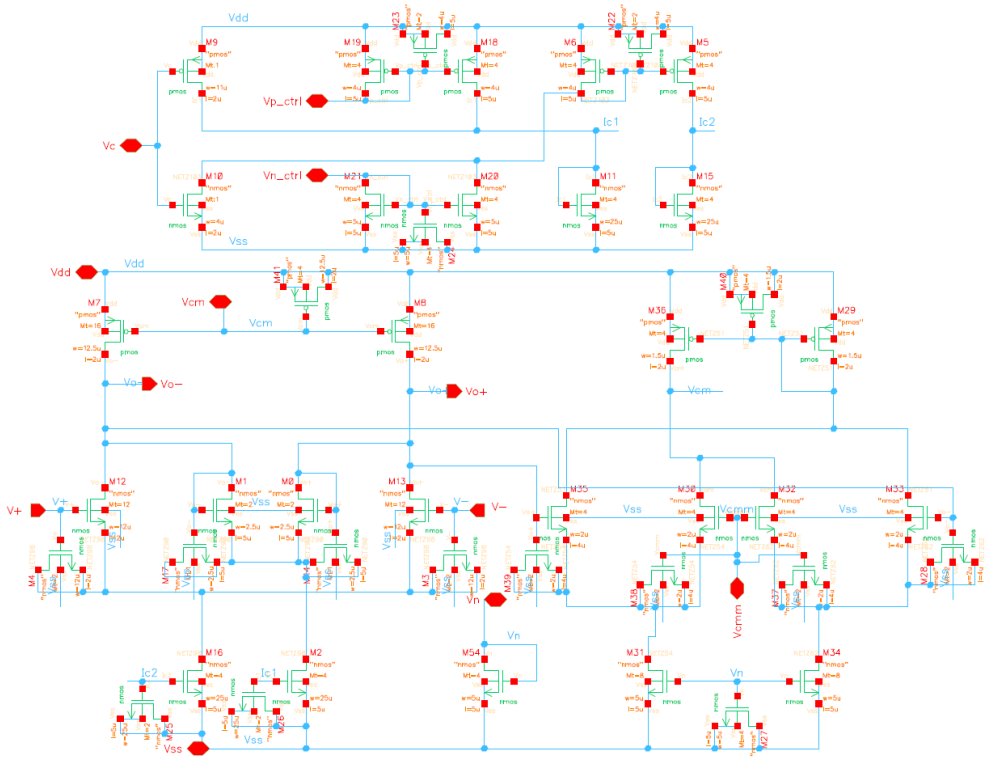


Figure 3.29: Transistor level circuit schematic of the implemented VGA.

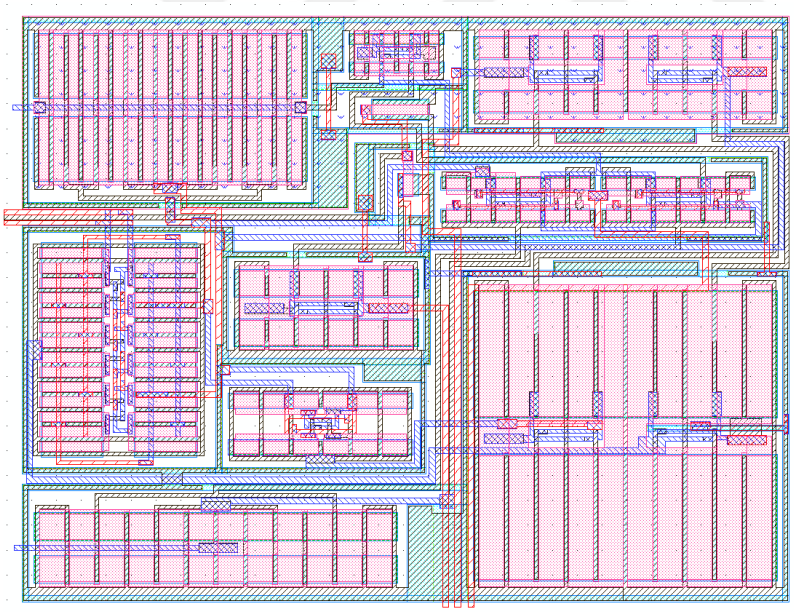


Figure 3.30: The layout of the implemented linear-in-dB VGA is shown in this figure.

The input and output signals are represented in Figures 3.32 and 3.33. The input signal is a sine wave with 30 mV peak value and 174.818 kHz frequency. Figure 3.32 represents the case when there is no filter at the output of the peak detector. The peak detector is just driving a $125k\Omega$ resistive load. However, Figure 3.33 is for the case when there is a low pass filter at the output of the peak detector ($C_{pd} = 25\ nF$ and

$R_{pd} = 125\ k\Omega$).

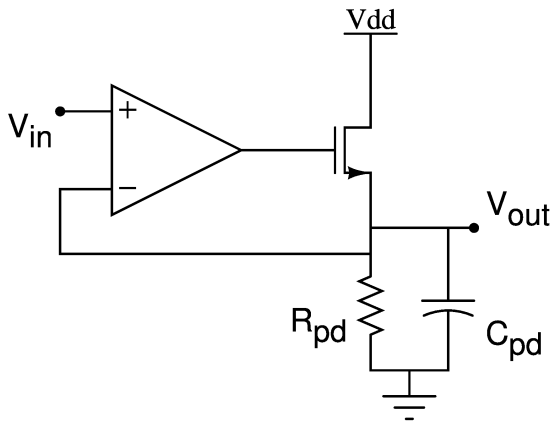


Figure 3.31: Circuit schematic of the peak detector.

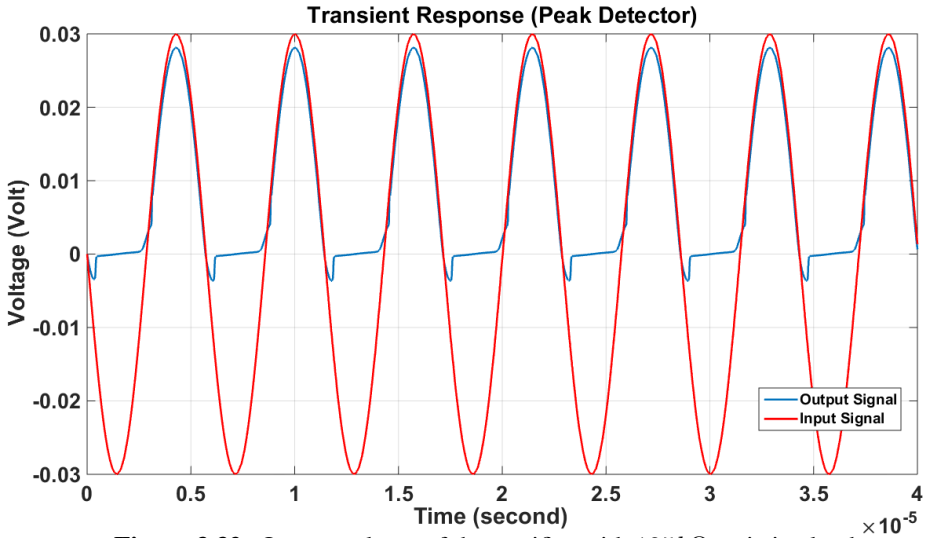


Figure 3.32: Output voltage of the rectifier with $125k\Omega$ resistive load.

The transistor level circuit schematic and the layout of the implemented peak detector are represented in Figures 3.34 and 3.35 respectively. An instrumentational amplifier is also implemented by the operational amplifiers in order to make it possible to detect the error between peak value of the signal and set point voltage. The instrumentational amplifier is shown in the closed-loop circuit in Figure 3.48.

3.3.4 TCF (Temperature Coefficient of Frequency) of the Electronic Circuitry

As mentioned before in chapter two, the DETF resonator used in this research has been designed and fabricated by Mr. Talha Köse in METU MEMS [4]. The TCF of

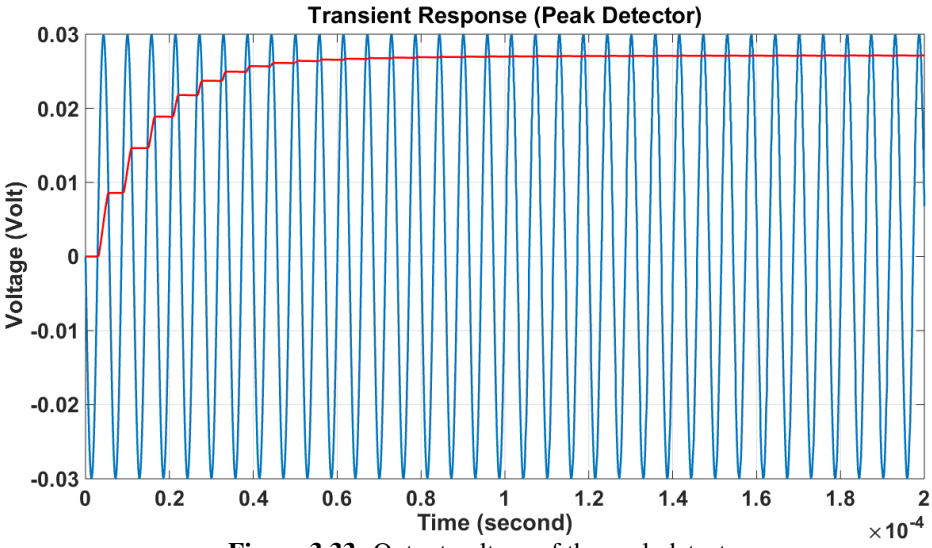


Figure 3.33: Output voltage of the peak detector.

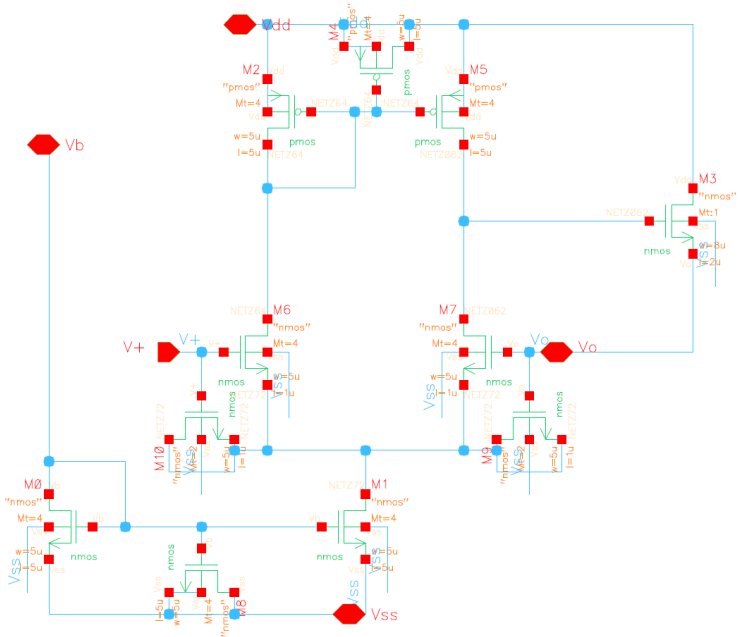


Figure 3.34: Schematic of the implemented peak detector.

his designed resonator is 53 ppm/K. sensitivity of the resonator will be determined by

$$\frac{df}{dT} = TCF \times f_{res} = 53 \times 10^{-6} \times 174818 \approx 9.27\ (Hz/K) \tag{3.17}$$

The sensitivity of the electronic circuitry to temperature is intended to be obtained. It has been done to evaluate the impact of electronic circuitry's TCF on the sensor sensitivity. To do this, it has been assumed that the resonator is not temperature

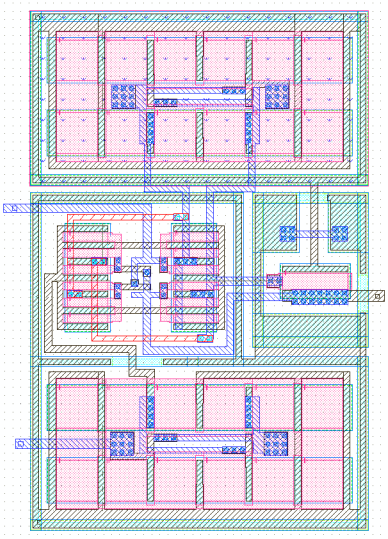


Figure 3.35: The layout of the peak detector.

dependent and only electronic circuitry determines the sensitivity of the sensor. Since it has been shown in Figure 2.15 that phase will determine resonant frequency as long as the resonator is operating in the tuning range, Equation 2.26 is used and the TCF of the electronic circuitry is derived when oscillator is operating at the steady state.

$$\Delta f = -\frac{f_{res}}{2Q}\Delta\phi$$

$$\frac{\Delta f}{f_{res}\Delta T} = -\frac{1}{2Q}\frac{\Delta\phi}{\Delta T} \tag{3.18}$$

AC analysis of the open-loop circuitry (the TIA and the VGA) is represented in Figure 3.36 for a temperature range of 80 degrees (from 0 °C to 80 °C). The AC analysis is done when the loop gain is one. The figure shows a gain change of 1.8 dB and phase change of 6.8 degrees (or equivalently 0.119 radians). It has been assumed that the resonator has no temperature sensitivity and only the electronic circuitry affects the resonant frequency. Therefore, the TCF of electronic circuitry might be achieved by

$$\frac{\Delta f}{f_{res}\Delta T} = \frac{1}{45704}\frac{0.119}{80} = 32.55 \times 10^{-9}\ or\ 32.55\ ppb/K$$

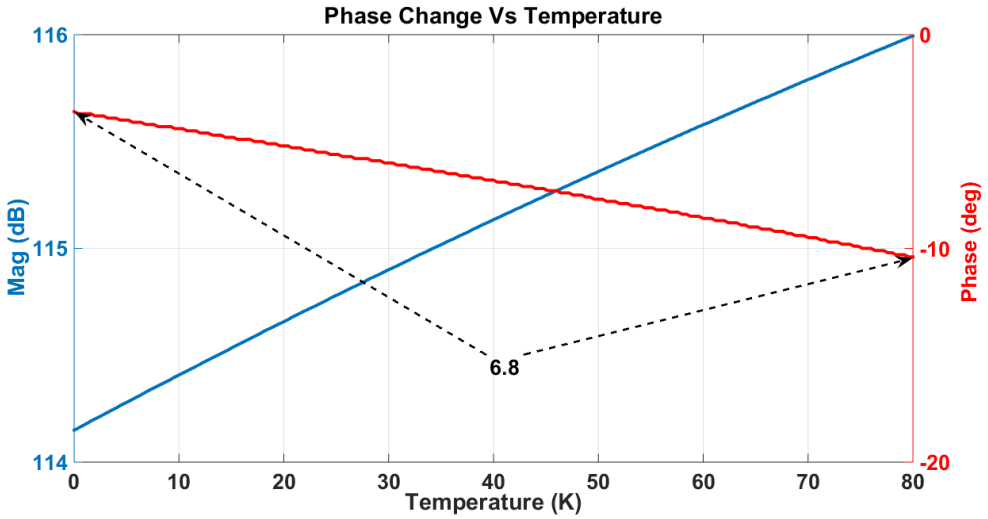


Figure 3.36: Phase change with respect to temperature change from 0 to 80 degrees.

The result mentioned above is obtained just to check the possible effect of the electronic circuitry on the sensitivity of the sensor. It has been achieved under a few assumptions. It shows that the electronic circuitry has less impact on the sensitivity of the sensor.

3.3.5 Obtaining PI Parameters of the AGC Loop (SIMULINK/MATLAB)

As shown in [54], at a steady state when the output voltage is stable, PI parameters of an AGC loop containing a linear-in-dB VGA can be calculated as shown in the following. Since

$$V_{out} = A_{VGA}V_{in} = \beta e^{\alpha V_C}V_{in} \tag{3.19}$$

output voltage change with respect to control voltage can be written by

$$\frac{dV_{out}}{dV_C} = \alpha\beta e^{\alpha V_C}V_{in} = \alpha V_{out} = \alpha V_{sp} \tag{3.20}$$

It implies that at the steady state condition, instead of Linear-in-dB VGA, a block with a gain equal to αV_{sp} can be placed in order to obtain PI parameters. This is shown in Figure 3.37.

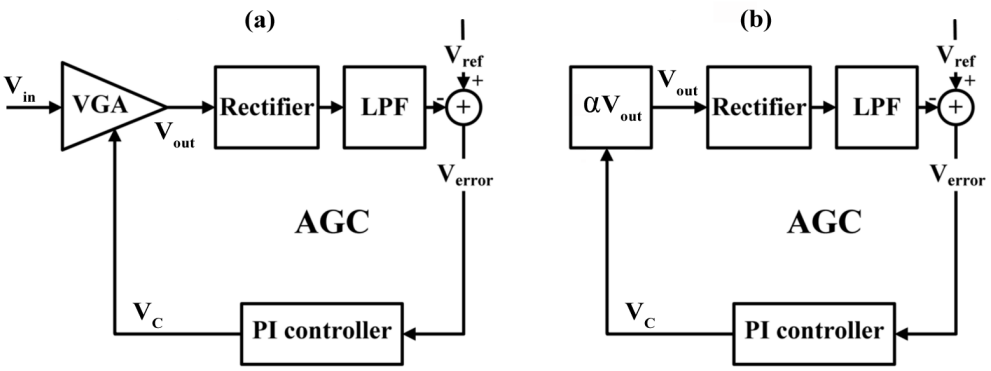


Figure 3.37: Simplified block diagram of the AGC block.

In the feedforward path, PI controller and VGA blocks exist. Therefore transfer function of the feedforward path can be written by

$$A(s) = \alpha V_{out} \frac{k_P s + K_I}{s} \tag{3.21}$$

And accordingly, for the feedback path which only contains a rectifier with a low pass filter (LPF), transfer function is determined by

$$\beta(s) = \frac{k_{pd}}{\tau_{pd} s + 1} = \frac{0.95}{3.125e-3s+1} \tag{3.22}$$

Transfer function of the whole block, V_{out}/V_{ref}, can be written as $A/(1+A\beta)$. To find the optimum PI parameters for the simplified AGC block, the AGC loop is constructed in SIMULINK/MATLAB as shown in Figure 3.38.

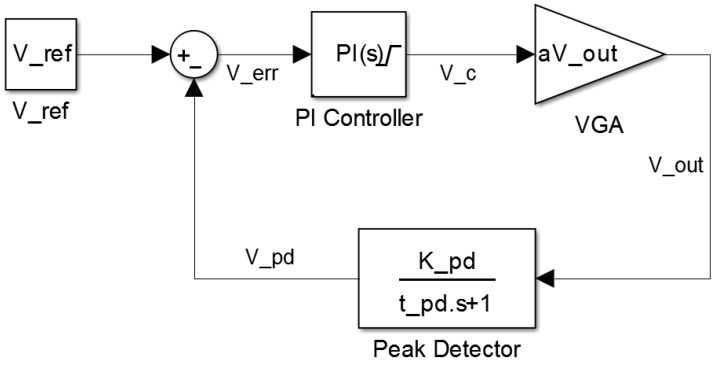


Figure 3.38: AGC loop constructed in SIMULINK/MATLAB to obtain PI parameters.

PI tuning can be done to obtain optimum parameters. Figures 3.39 and 3.40 represent step and Bode plot of the AGC loop.

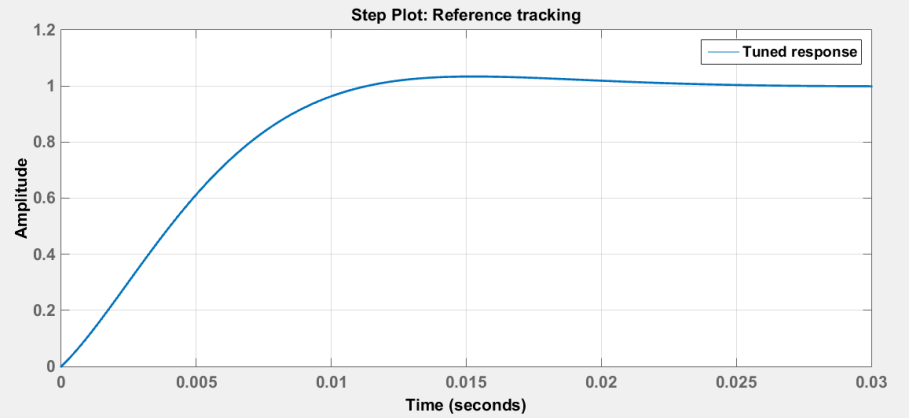


Figure 3.39: Obtained step response of the constructed AGC loop.

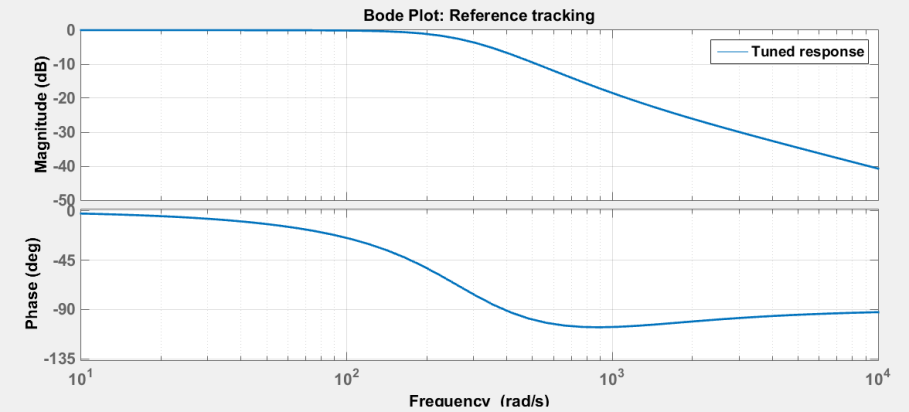


Figure 3.40: Obtained Bode plot for the constructed AGC loop.

The tuner gives less than $20\ ms$ settling time and $7.6\ ms$ rise time. Overshoot is about 3.4% and Phase margin is 70.8 degrees. By using DETF and TIA transfer function from Equation 3.6 and using VGA gain equation from Equation 3.16, the loop can be constructed in SIMULINK/MATLAB as shown in Figure 3.41. Gain of DETF and TIA has changed because the effect of high pass filter and TIA itself is taken into account in Equation 3.6. The simulation results of the constructed loop in SIMULINK/MATLAB are represented in Figure 3.42. Table 3.4 also summarizes the specifications of the components in the AGC block.

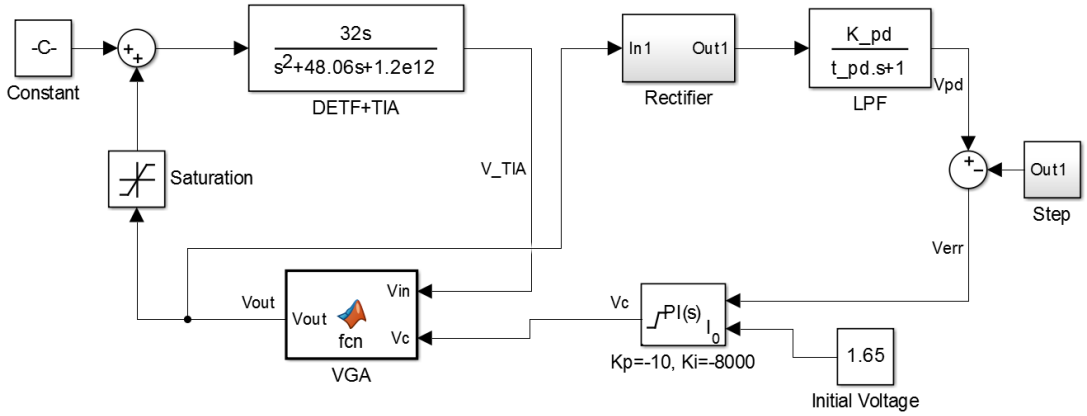


Figure 3.41: The sensor constructed in SIMULINK/MATLAB to check the performance of the AGC block and the obtained PI parameters.

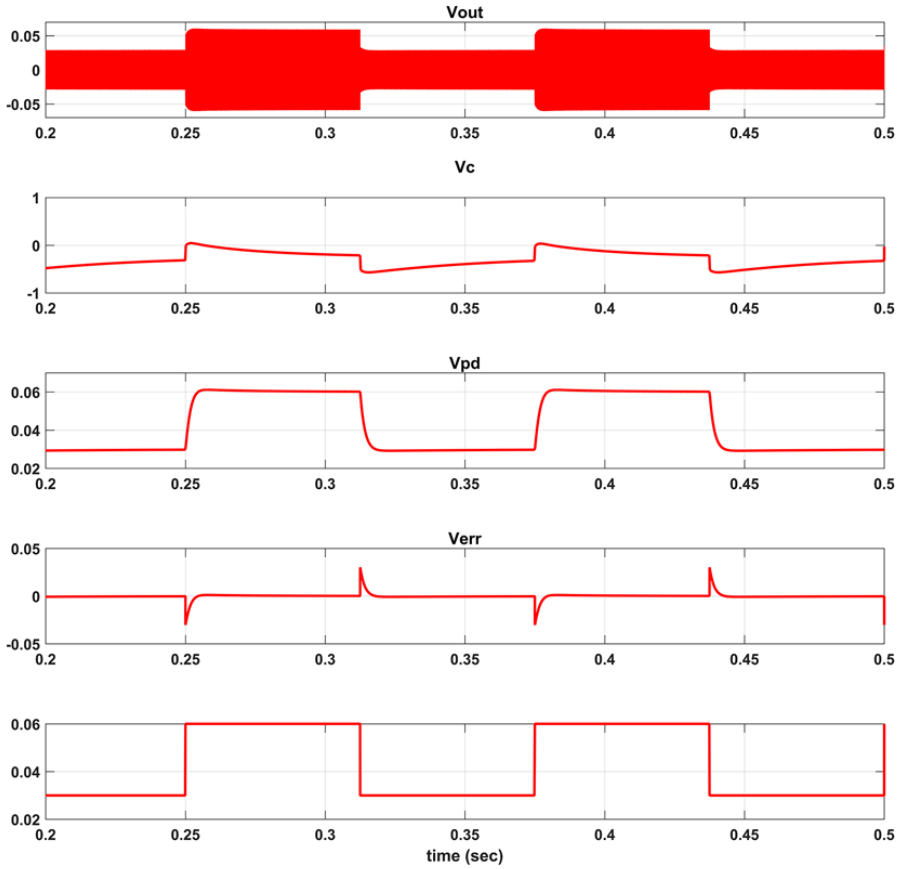


Figure 3.42: The simulation results for the constructed loop in SIMULINK/MATLAB is represented in this figure.

Table 3.4: The specifications of the components in the AGC block.

VGA			
BW (V_C=1.6 V)	640 kHz	**BW (V_C=-0.65 V)**	2 MHz
Area	118.2 µm×154.7 µm	**Power Dissipation (V_C=-0.65 V)**	800 µA
Gain Range	23.5/1.3 dB/V	**Power Supply**	±1.65
Amplitude Detector			
R_{LPF}	125 kΩ	**C_{LPF}**	25 nF
Area	63.5 µm × 41.3 µm	**Power Dissipation**	24 µA
PI Controller			
K_I	-10	**K_P**	-8000

3.3.6 Noise and Gain Performances of the Closed-loop Circuit at Start-up and Steady-state

At start-up, control voltage (the output voltage of PI controller, V_c) is at its maximum (about $1.6\ V$). With $V_c = 1.6$, VGA gain is saturated to $22.11\ dB$. The oscillation will start by the help of noise and will finally be stabilized at a control voltage close to $-600\ mV$.

As represented in Figure 3.27, the output referred voltage noise of the VGA has the minimum contribution to the overall output referred voltage noise (noise contribution of the TIA is included). The noise contribution of VGA even at its minimum gain is smaller than the noise contribution of TIA to the overall output voltage noise. This is represented in Figure 3.43. This figure shows that the output referred noise of the open-loop circuitry at 174.818 kHz is mostly due to the TIA amplifier and is equal to $102\ nV/\sqrt{Hz}$.

The full dynamic range of the VGA is used to obtain loop gain equal to 15.36 at start-up and one at steady state (Figure 3.44). In addition, noise is at its maximum at the beginning which will help to achieve a quick start-up, it becomes minimum at lower control voltages as shown in Figure 3.45. Output referred voltage noise of the open-loop electronic circuitry with respect to temperature is also represented in Figure 3.46.

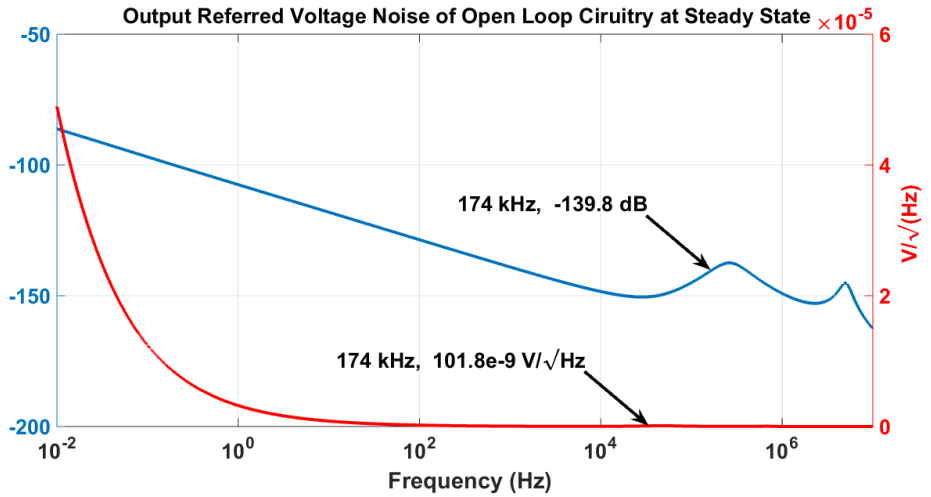


Figure 3.43: Open-loop output referred voltage noise.

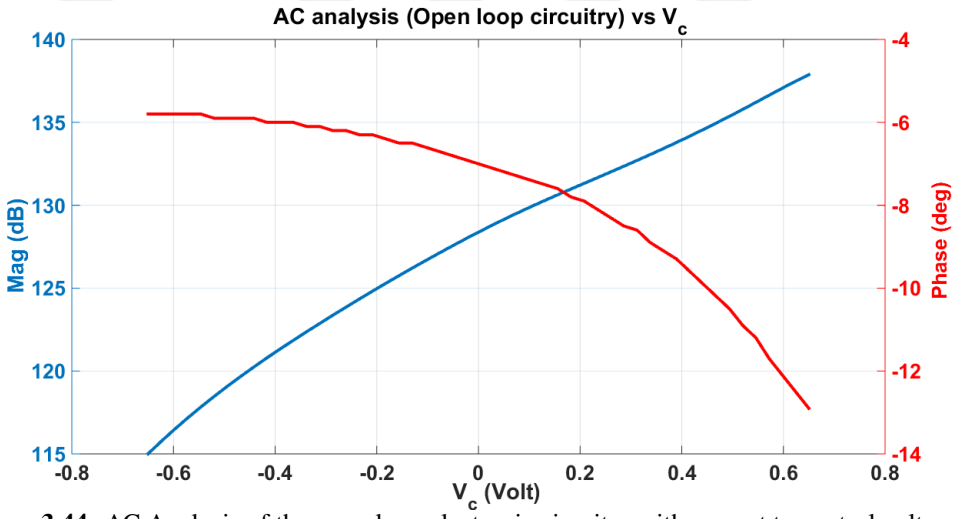


Figure 3.44: AC Analysis of the open-loop electronic circuitry with respect to control voltage.

3.3.7 Phase Noise Prediction of the Closed-loop Circuit

As shown in the previous chapter, after start-up a carrier will rise from noise at $174.818\ kHz$. Noise around this carrier will determine the noise floor of output signal which is called the additive noise. The noise around the frequency of $174.818\ kHz$ is about $101.8\ nv/\sqrt{Hz}$ or equivalently $-139.85\ dB$. The output rms voltage is also 22 mV (30 mV(P-P)). Far-from-carrier for the single sideband phase noise is predicted to be about

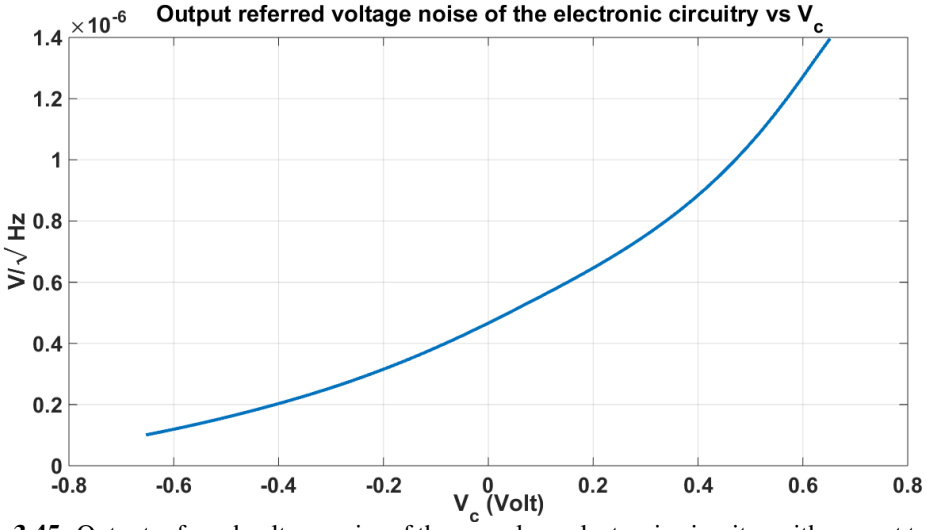


Figure 3.45: Output referred voltage noise of the open-loop electronic circuitry with respect to control voltage.

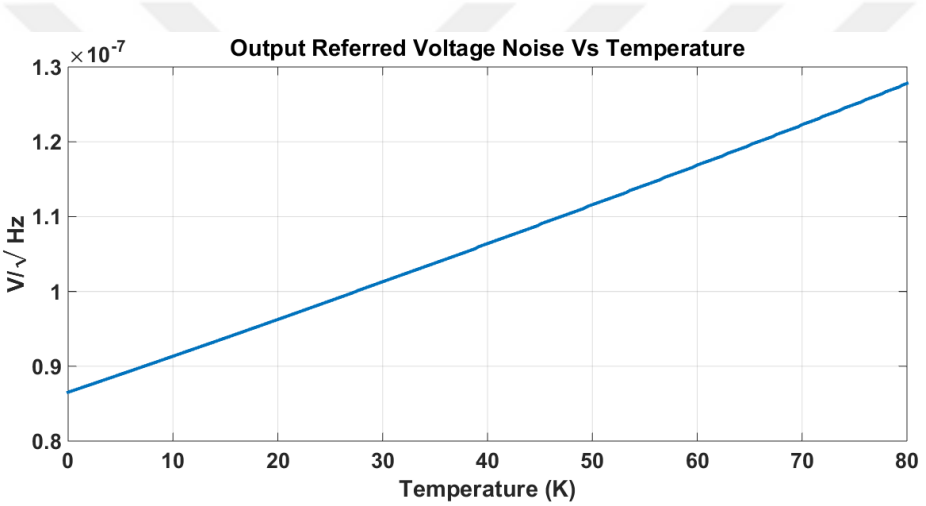


Figure 3.46: Output referred voltage noise of the open-loop electronic circuitry with respect to temperature (at steady state).

$$\begin{aligned} L_{far}(f_m) &= 20log(\frac{V_{noise}(V/\sqrt{Hz})}{V_{out,rms}(V)}) \\ &= 20log(\frac{101.8e-9}{22e-3}) = 20log(4.63e-6) \\ &\approx -107\,(\frac{dBc}{Hz}) \end{aligned} \tag{3.23}$$

As previously shown in Figure 2.23, the Phase noise would have f^0, f^-1 and f^-3 components. Since "What the analog circuit design environment plots as phase noise is really the total noise scaled by the power in the fundamental oscillation mode"

[46], flicker noise of Figure 3.43 will get divided by the voltage in the fundamental frequency ($22\ mV$) as well. Or equivalently it will rise by $33.15\ dB$ as represented in Figure 3.50.

Leeson frequency is also obtained to be $f_L = f_{res}/2Q = 174818/46000 \approx 3.8Hz$. For frequencies smaller than $3.8\ Hz$, phase noise profile will be f^{-3}. The Leeson frequency in Figure 3.50 is much smaller than the predicted value because the flicker noise is also divided by the rms voltage at the oscillation frequency as well which is not in consistent with what is offered by Lesson equation [6].

3.3.8 Transient Response and Phase Noise of the Closed-loop Circuit (Cadence)

Finally, the closed-loop circuit and the implemented layout are represented in Figures 3.48 and 3.47 (or 3.49) respectively. Additional pads are used to provide access to the operational amplifiers. By doing this, the operational amplifiers can be used as either buffer or second order filter in the loop when feedthrough cancellation is not done.

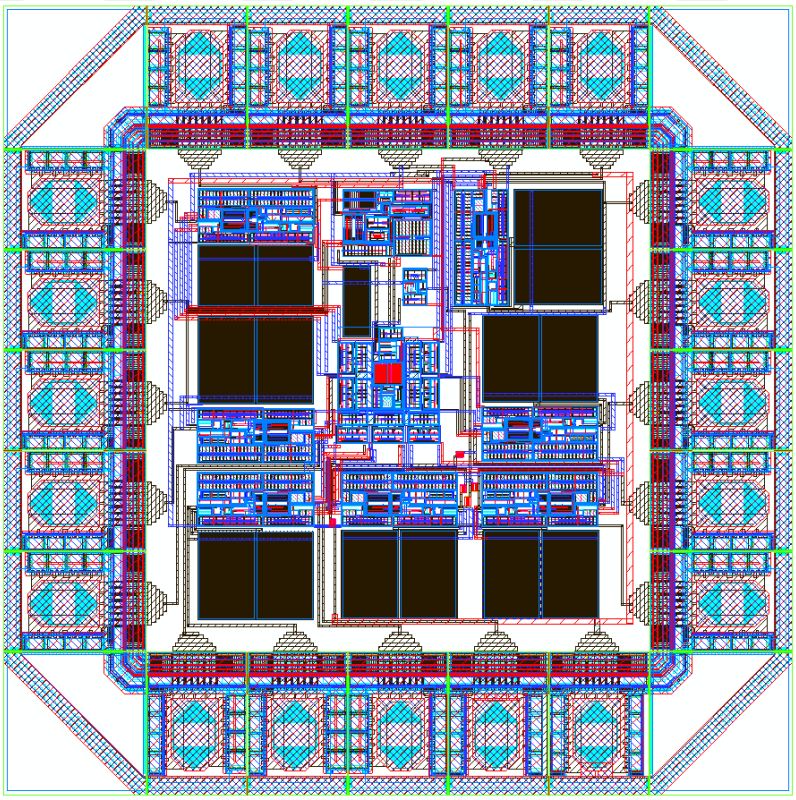


Figure 3.47: Implemented layout of the closed-loop circuit with the AGC block.

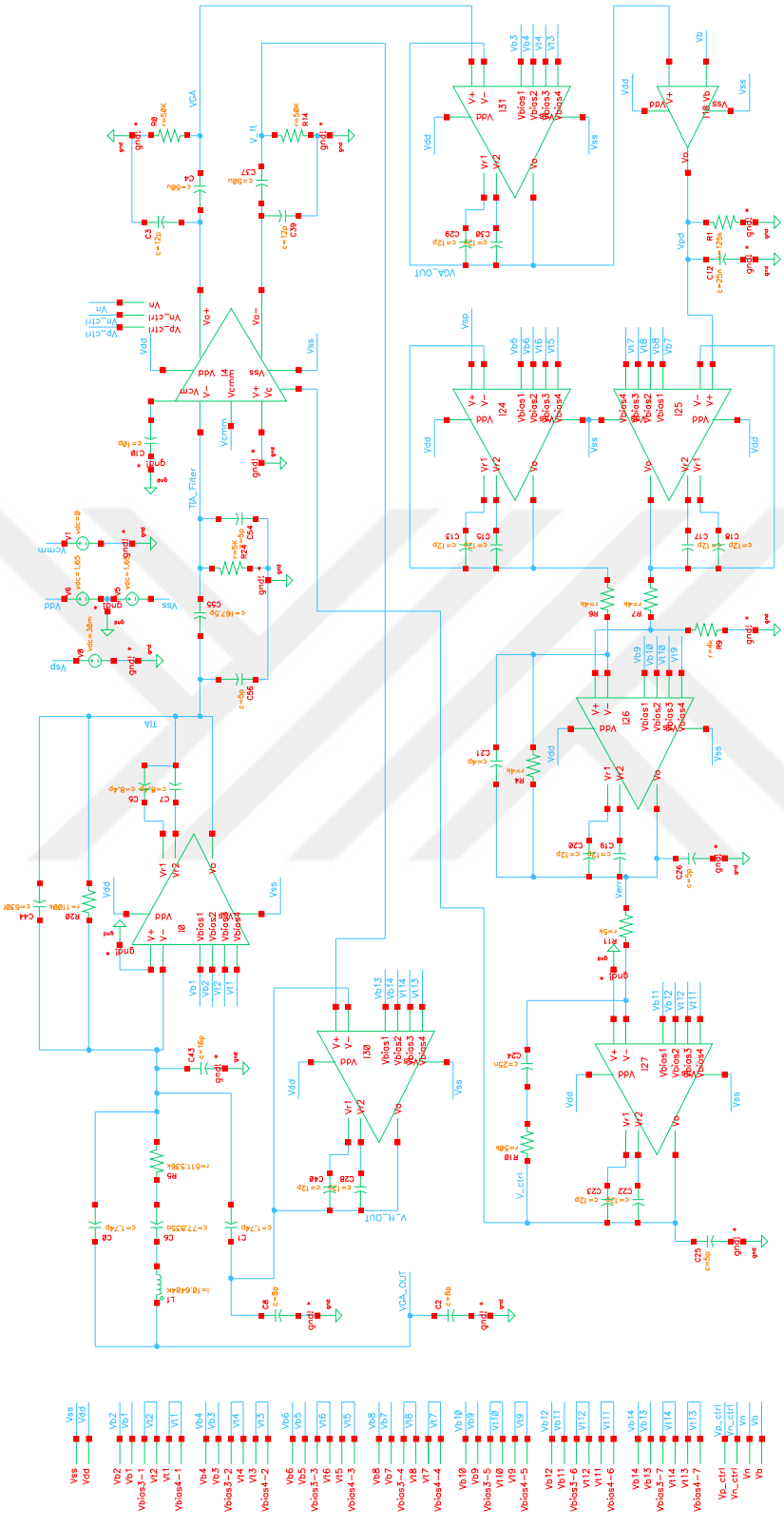


Figure 3.48: The closed-loop circuit with an AGC block.

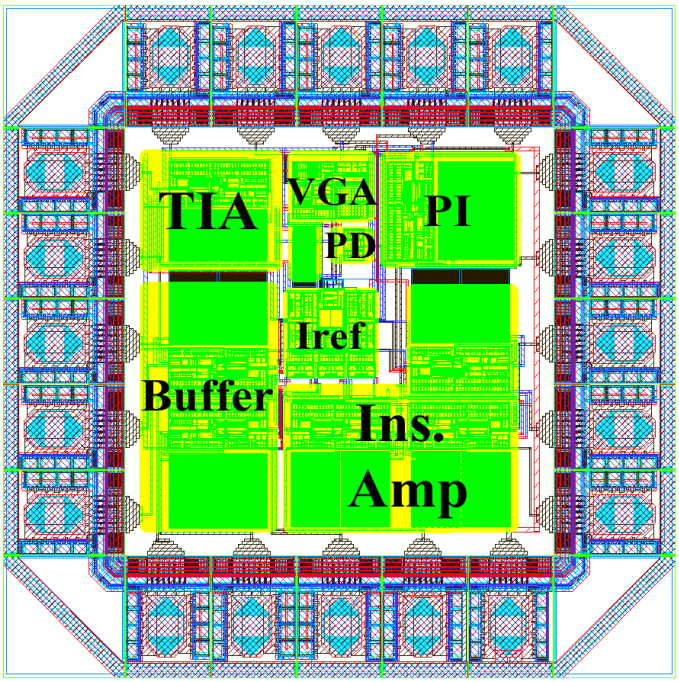


Figure 3.49: Different components represented in the layout of the integrated circuit.

After closing the loop as shown in Figure 3.48, transient analysis is accomplished for two different set points: 30 mV and 60 mV peak-to-peak voltages. The results are shown in Figure 3.51. The first overshooting is due to the control voltage, it is at its maximum, and it takes some time to reach a steady state. Phase Noise obtained from Spectre/Cadence, PSS and PNoise analyses, is shown in Figure 3.52. It behaves according to what is predicted in section 3.3.7.

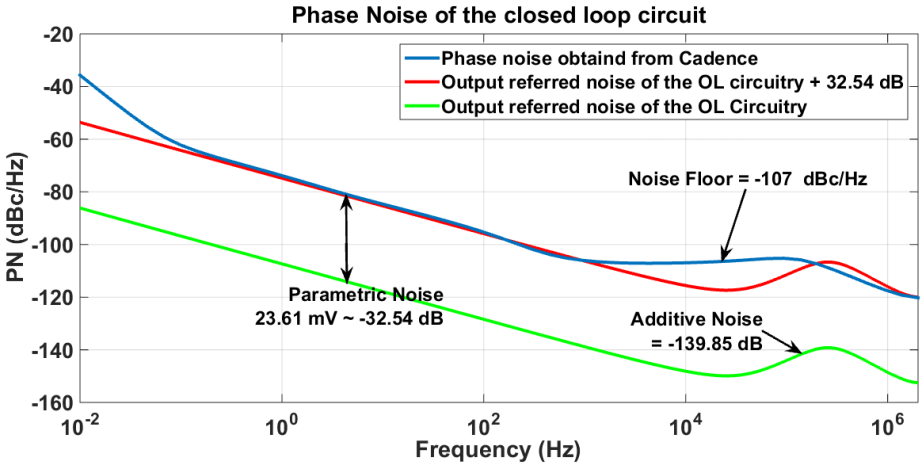


Figure 3.50: Phase Noise of the closed-loop circuit along with the noise performance of open-loop circuitry are represented in this figure. Frequency range of the phase noise measurement is relative.

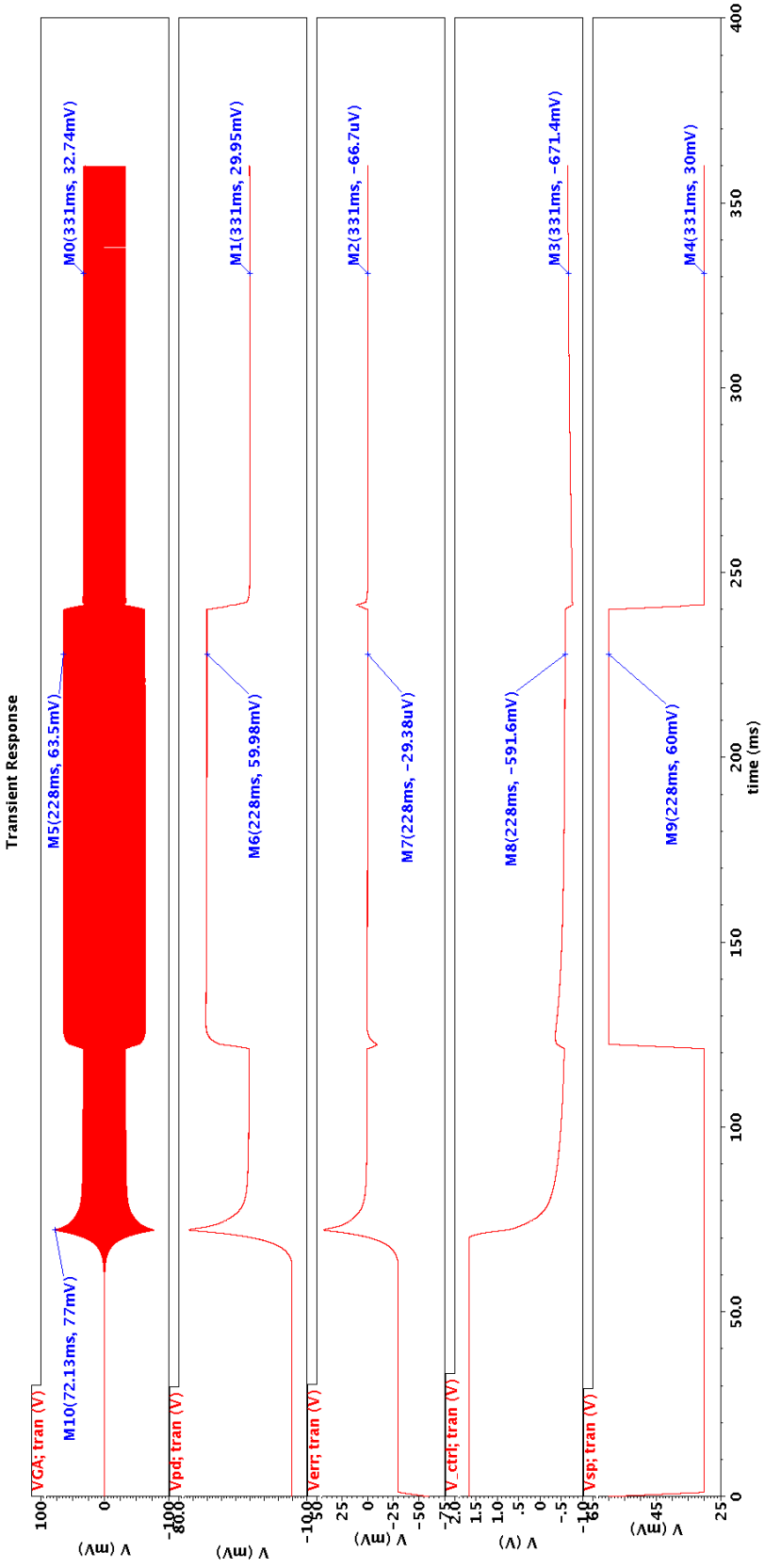


Figure 3.51: Transient response of the closed-loop circuit at steady state.

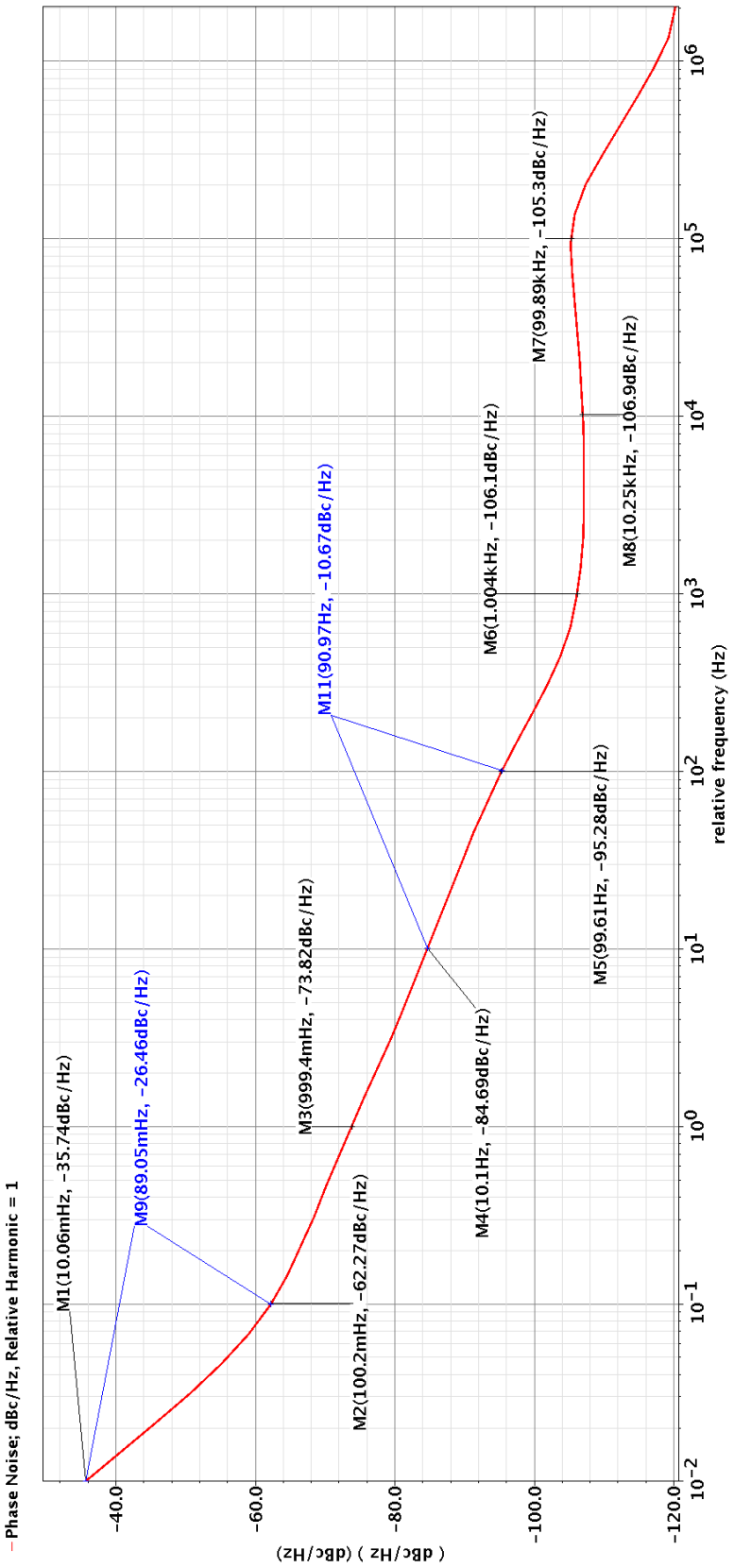


Figure 3.52: Phase noise response of the closed-loop oscillator at steady state.

The area of the implemented integrated circuit is 1374.5 μm$\times$1374.5 μm and the current drawn from the power supply ($\pm$1.65 V) is 3.3 mA.

3.3.9 Resolution of the Sensor

As previously shown in section 2.5.2.4, sensor resolution [3] can be represented by

$$Sensor\ \ resolution\ =\ \frac{frequency\ \ resolution}{sensitivity\ \ of\ \ the\ \ sensor} = \frac{\sqrt{\int f_m^2\ \ \phi(f_m)\ \ df_m}}{\frac{df}{d(Quantity)}}$$

Resonator sensitivity is also calculated by Equation 3.17 as shown below

$$\begin{aligned} \frac{df}{dT} &= TCF \times f_{res} = 53 \times 10^{-6} \times 174818 \\ &\approx 9.27\ (Hz/K) \end{aligned}$$

The double sideband phase noise ($\phi(f_m)$) is also equal to two times of the single sideband phase noise, $\phi(f_m) = 2 \times L(f_m)$. Additionally, if white phase and flicker phase noise sources (Figure 3.52) are only considered to be at phase noise spectrum, the phase noise can be written as

$$L(f_m) = 20 \times 10^{-12} + \frac{41.5 \times 10^{-9}}{f_m} \tag{3.24}$$

If only white phase noise source has been filtered out the only remaining noise will be flicker phase noise source. With bandwidth up to approximately 1kHz, the sensor resolution is achieved to be

$$\begin{aligned} Sensor\ \ resolution\ &= \frac{\sqrt{2(41.5 \times 10^{-9}) \int f_m\, df_m}}{9.27} \\ &= 0.02198^{\circ}C \end{aligned} \tag{3.25}$$

3.4 Conclusion

Closed-loop readout circuit with an AGC block is constructed in XFAB 0.35μm CMOS Process in this chapter. The goal of the loop implementation is to reduce the far-from-carrier and close-to-carrier phase noise components as much as possible. It has been shown in this chapter that the VGA has the dominant effect on the flicker (close-to-carrier or parametric) noise performance of the loop. On the contrary, the input referred voltage noise of the operational amplifier along with the input parasitic capacitance determine the thermal (far-from-carrier or additive) noise performance of the loop.

If a few stages of VGA could be used in the loop to increase the gain range, the gain of trans-resistance amplifier could be increased and consequently better SNR could be achieved. Employing two or three stages of VGA in the loop is limited by the flicker noise performance of the VGA, due to the fact that adding stages in series will increase output flicker noise considerably. Reducing the flicker noise of the VGA can be considered as the future work.

Phase noise obtained in section 3.3.8 is in consistent with [3] since the noise profile (white noise and flicker noise) is scaled by the oscillation signal. While according to [6], flicker noise portion should not be signal power dependent. That's the reason why Leeson frequency is smaller than the calculated value (3.8 Hz).

Because of the fact that the obtained results are from the simulations in Cadence, it is possible that the resonator affects the close-to-carrier phase noise components once integrated with the electronic circuitry. That's the reason why only "white phase" is filtered out in sensor resolution calculation. As it will be shown in the next chapter, when sensor resolution is intended to be calculated by using Allan deviation, "white phase", "flicker phase" and "white frequency" averaging are used to get rid of these noise sources and that's one of the reasons why the obtained result from discrete components give better resolution.

CHAPTER 4

IMPLEMENTING CLOSED-LOOP CIRCUIT WITH DISCRETE COMPONENTS

4.1 Discrete Component Based Closed-loop Design

To verify the functionality of the implemented closed-loop circuit in CMOS technology, the circuit is again constructed by discrete components in this chapter. The goal is to construct the loop, then analyze the stability of that. Of course to assess the noise and phase noise performances of the constructed loop, a phase noise measurement setup could be built up, but since Allan deviation was available to assess the stability and the resolution of the sensor, the phase noise measurement setup implementation is also considered as the future work.

The design procedure is the same as the one in CMOS Technology. Each block is constructed and tested in LTSpice. The PI parameters of the AGC loop is obtained in SIMULINK/MATLAB. At the end, after verification of the closed-loop circuit by LTSpice and MATLAB, it is laid out on a PCB board and examined for functionality. Because of the fact that the same procedure is employed here, the details are not brought up again.

4.1.1 Operational Amplifier - AD8606

AD8606 operational amplifier is used as the core of tran-simpedance amplifier and since it is a unity gain stable op-amp, it is used as the buffer and voltage amplifier in the loop as well. AD8606 has smaller than 7 $nv/\sqrt{Hz}$ input referred voltage

noise at $174.818\ kHz$ and about $10\ MHz$ unity gain bandwidth. According to its noise performance, corner frequency of this op-amp is much smaller than the corner frequency of the op-amp implemented in the previous chapter in CMOS technology. This is an advantage for this op-amp that if the flicker noise of the VGA and other stages in the loop have smaller PSDs, then the whole close-to-carrier phase noise of the loop might have a better performance compared to the implemented closed-loop circuit in CMOS Technology.

4.1.2 Trans-impedance Amplifier

By taking variable gain amplifier's dynamic range into account, the gain of the TIA amplifier (high pass filter and feedback capacitor are included in the gain calculation) is selected to be around $168\ k\Omega$. The feedback resistor and capacitor are chosen to be $200\ k\Omega$ and $3.35\ pF$ in order to obtain a TIA with quality factor of 0.36 (over-damped). The 3dB bandwidth and the output rms noise (section 2.2.3) of the TIA are obtained to be $266\ kHz$ and $55\ \mu V$. Phase error at the $174.818 kHz$ is about 39 degrees, and the gain of the TIA would not have any peaking since its quality factor is much smaller than 0.7. Trans-impedance amplifier is shown in Figure 4.5 and its corresponding gain is represented in Figure 4.1.

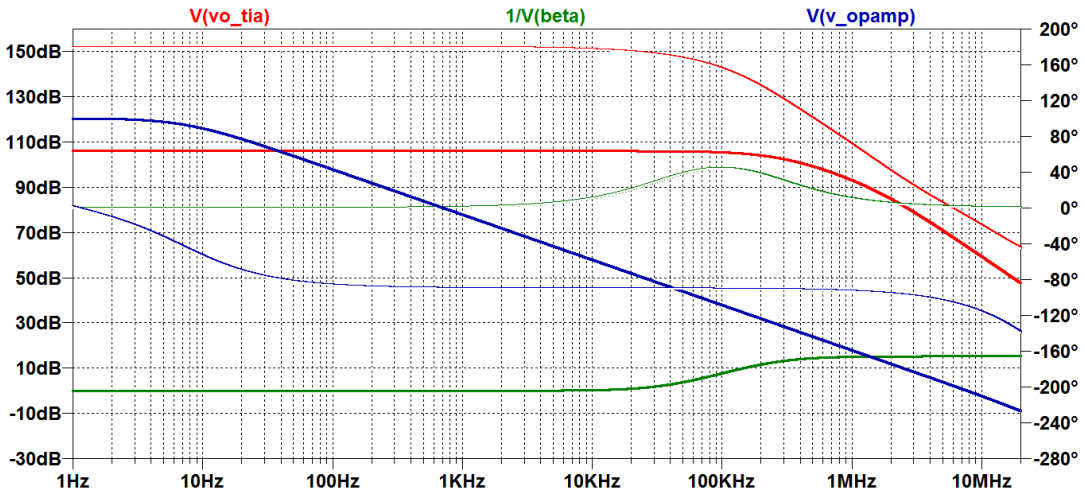


Figure 4.1: TIA Stability Analysis.

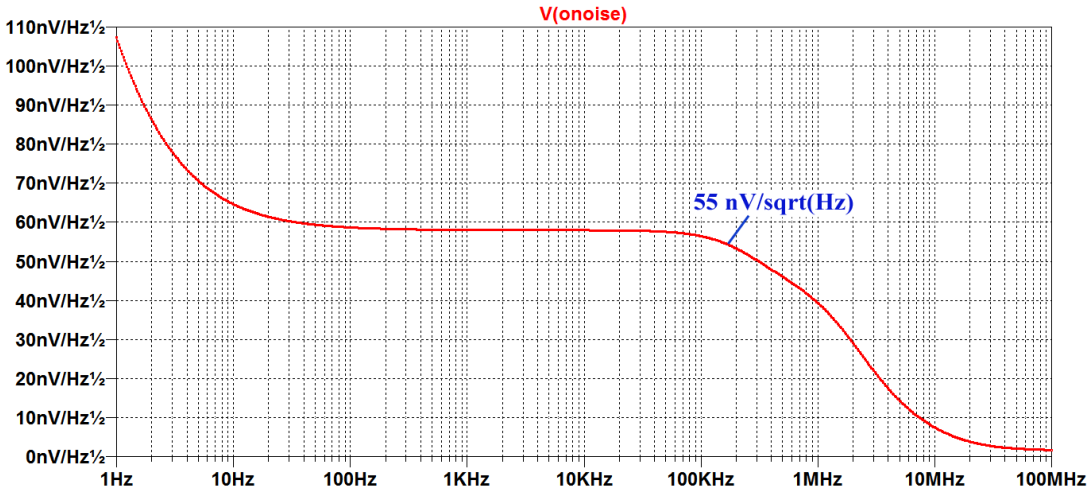


Figure 4.2: Output referred voltage noise of the TIA amplifier.

4.2 Automatic Gain Control Loop

Automatic gain control block consists of an AD604 variable gain amplifier, AD630 modulator (used as the rectifier and peak detector), AD8222 instrumentational amplifier (as the error detector) and PI controller (implemented by AD8606).

4.2.1 Linear-in-dB Variable Gain Amplifier - AD604

AD604 is a Linear-in-dB variable gain amplifier with $0.8\ nV/\sqrt{Hz}$ input referred voltage noise and 0 to 48 dB gain range. Its input resistance and capacitance are $300\ k\Omega$ and $8.5\ pF$ respectively. Input common mode range is $\pm 0.4\ V$. Control voltage for the gain range of 48 dB is from 0 V to 2.5 V. Finally, its 3dB bandwidth is 40 MHz.

A second order low pass filter will be used at the output to limit its bandwidth. The gain equation is given below

$$Gain(dB) = 20(dB/V) \times VGN(V) - 5(dB) \tag{4.1}$$

or equivalently can be written as

$$\begin{aligned} Gain &= 0.56 \times 10^{VGN} \\ &= 0.56 \times e^{2.3VGN} \end{aligned} \tag{4.2}$$

where VGN is the control voltage of the variable gain amplifier.

4.2.2 Peak Detector, Low Pass Filter, Error Detector and PI Controller

AD630 is a high precision balanced modulator/demodulator. The full bandwidth of this modulator is 350 kHz. This modulator is used as a full wave rectifier in automatic gain control block. A low pass filter will be used after this modulator to extract its DC value. The output DC voltage will be equal to $2/\pi$ multiplied by the peak value of rectified signal.

AD8222 instrumentational amplifier is used as the error amplifier. Its 3dB bandwidth is 1MHz when the gain is unity. It is employed in the AGC loop to detect the error between the set point and the DC voltage of the rectifier. PI controller is also implemented by AD8606 operational amplifier as will be shown in the next sections.

4.3 Obtaining PI Parameters of the AGC Loop (SIMULINK/MATLAB)

PI parameters of the automatic gain control block have been obtained for CMOS based readout circuit in section 3.3.5. Since we have a linear-in-dB VGA, we can repeat the same procedure for obtaining PI parameters of a closed-loop with discrete components as well.

The set point or reference voltage for the closed-loop circuit with discrete components is set to 16 mV. This is equivalent to $(0.016\pi)/2$ peak voltage or $(0.016\pi)/(2\sqrt{2})$ rms voltage. α of the variable gain amplifier as shown in section 4.2.1 is equal to 2.3. Thus the PI parameters for a set point voltage of $(0.016\pi)/2$ are obtained to be $k_p = -14$ and $k_i = -66667$.

4.4 Noise and Gain of the Closed-loop Circuit at Start-up and Steady-state

At the start-up, the output voltage of PI controller is at its maximum, 2.5V. The VGA will also provide its maximum gain, 40 dB, as shown in Figure 4.3. This figure also represents the steady state gain when the output signal is equal to 25.2 mV peak voltage.

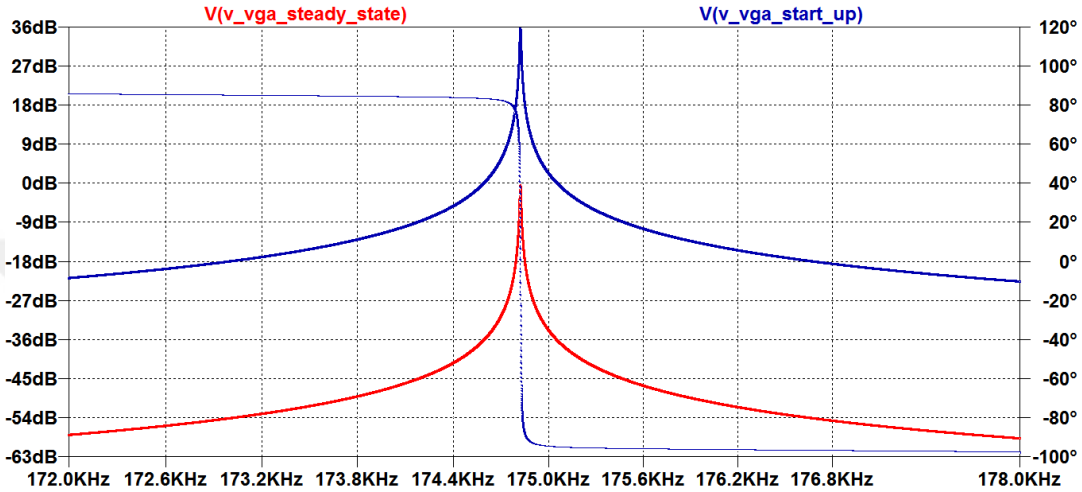


Figure 4.3: Start-up and steady-state AC Analyses.

Output referred voltage noise at the steady state ($V_c = 1.4\ V$ and $V_{out} = 25.2\ mV$ peak voltage) is given in Figure 4.4. This amount of noise can be considered as the approximate value for the noise floor of the closed-loop phase noise.

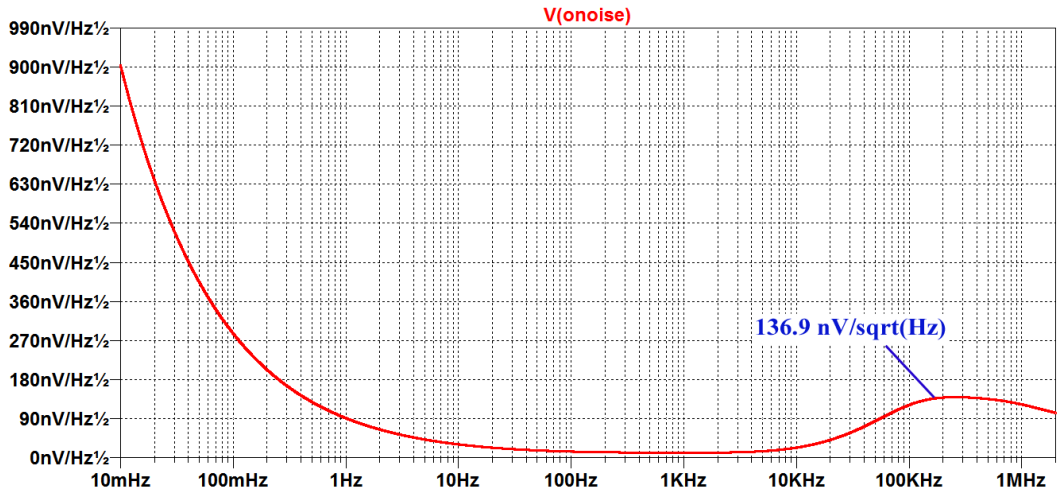


Figure 4.4: Output referred voltage noise of the open-loop circuitry.

4.5 Implemented Loop in LTSpice

Figure 4.5 represents the implemented closed-loop circuit in LTSpice. Figure 4.6 also shows transient response when set point voltages changes from 25.2 mV to 55 mV (peak voltages).

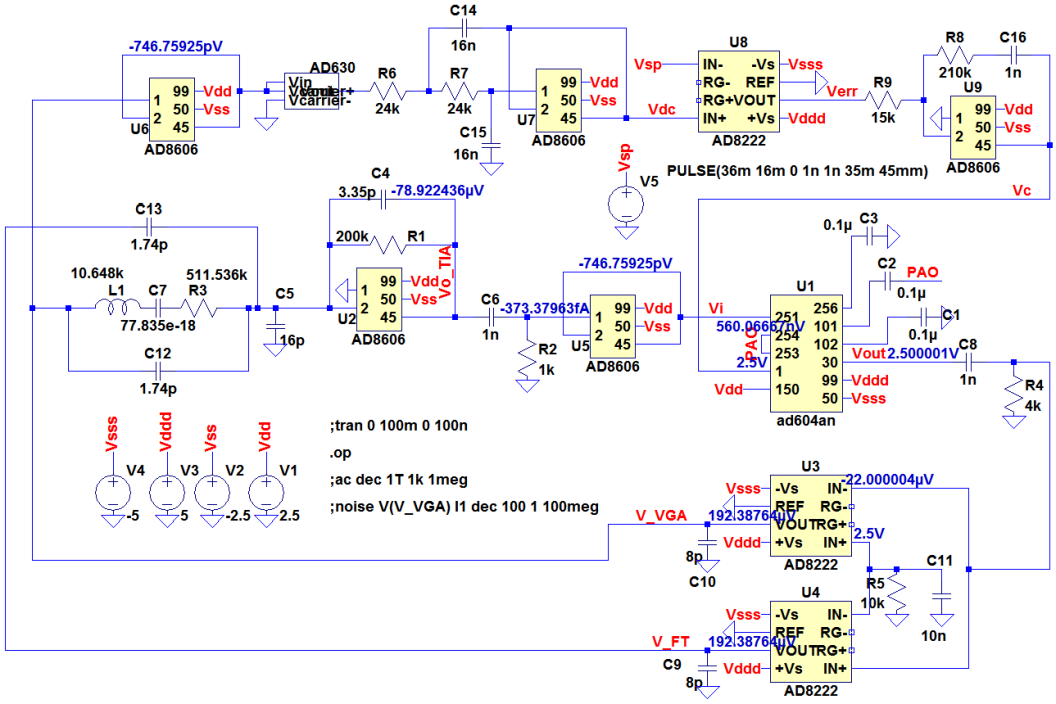


Figure 4.5: The closed-loop implemented by discrete elements.

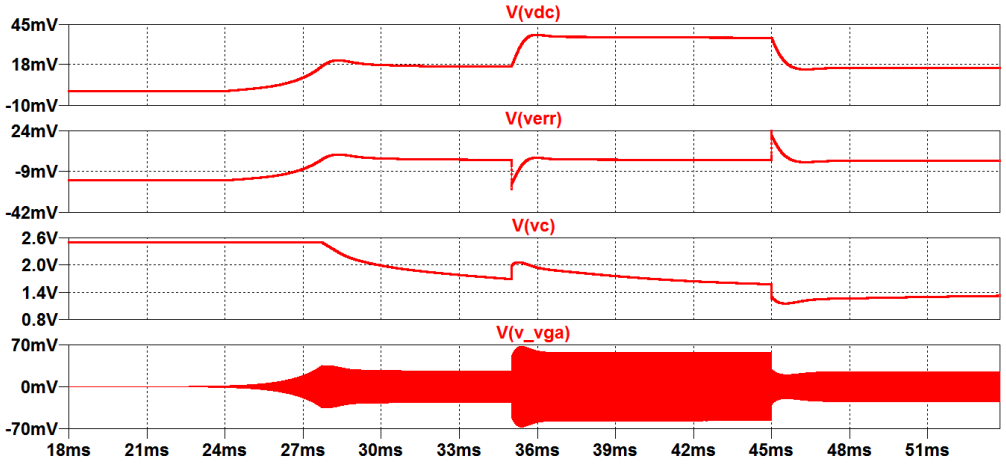


Figure 4.6: Transient response of the closed-loop circuit simulated in LTSpice.

4.6 Test Setup

The closed-loop circuit is implemented with commercial surface mount devices on a reliable PCB. The designed PCB is shown in Figure 4.7. Also Figure 4.8 represents the PCB with all discrete components mounted. The PCB has been designed to be used with two resonators, to make it possible to do feedthrough cancellation. However, due to the fact that there were a limited number of resonators, the feedthrough cancellation is not employed. A second order loop pass filter added in series with the variable gain amplifier to limit the bandwidth and provide enough phase shift to compensate the phase change made by the feedthrough current.

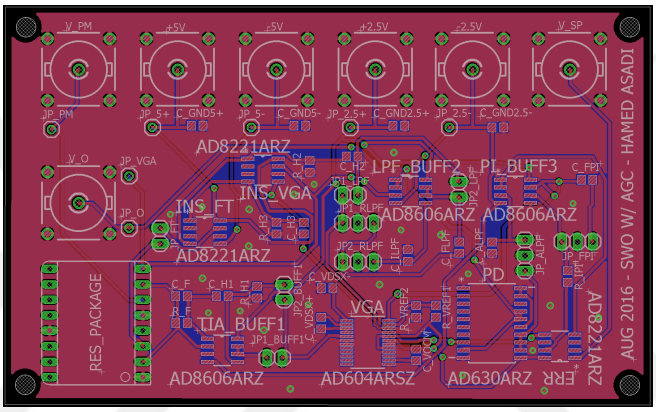


Figure 4.7: Printed circuit board of the closed-loop circuit.

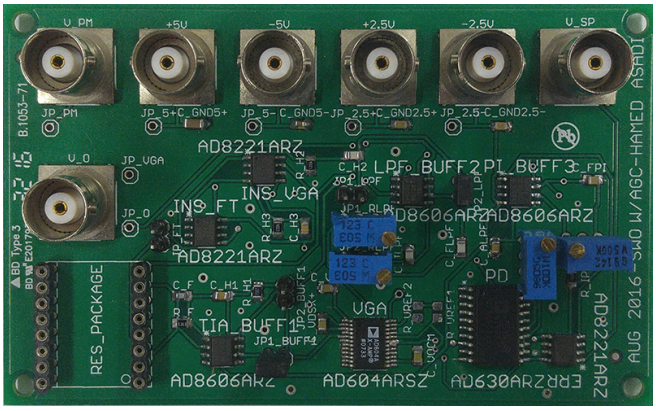


Figure 4.8: Printed circuit board of the closed-loop circuit with discrete components mounted.

Figure 4.9 shows the test equipment used to verify functionality of the sensor. Data acquisition is done for an hour for 21814 samples of data at room temperature. Obtained frequency data is represented in Figure 4.10, Allan deviation corresponding to the obtained frequency data is also shown in Figure 4.11. Bias instability for this

sensor is measured to be 0.0045°C for an averaging time of 5.28 seconds.

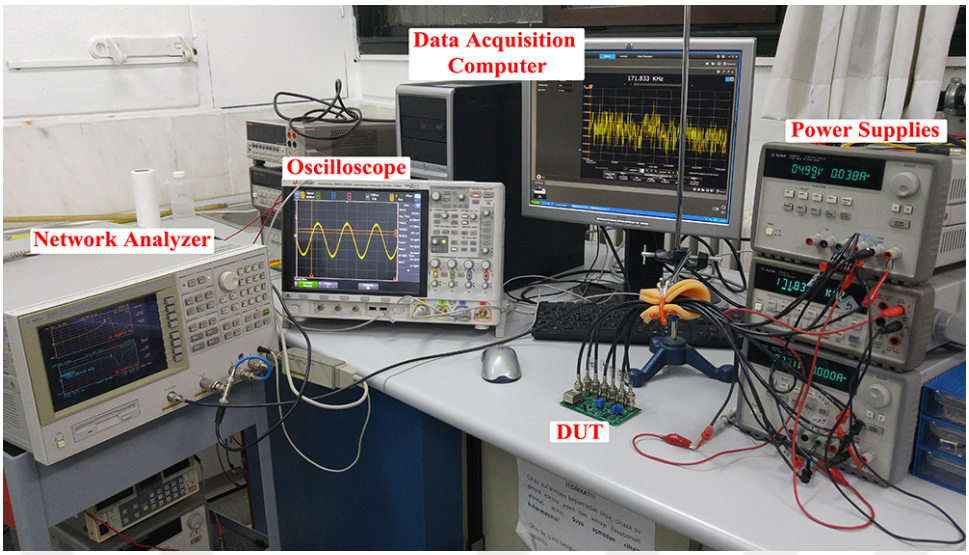


Figure 4.9: Test setup used for characterization of the implemented closed-loop circuit.

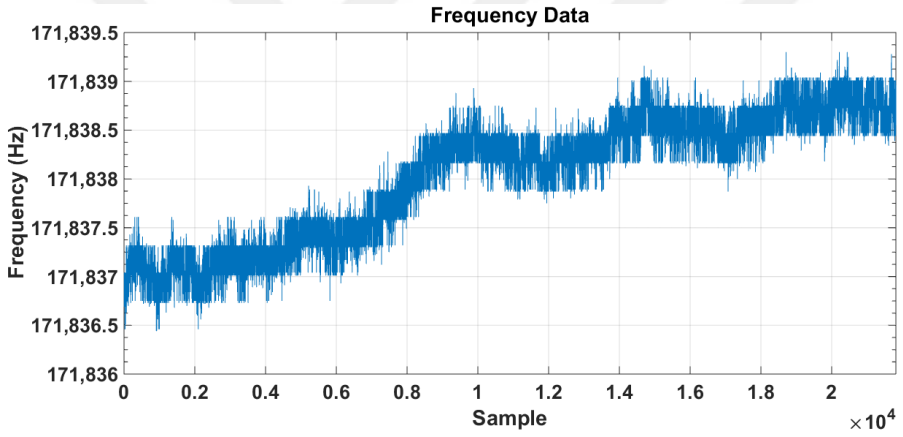


Figure 4.10: Frequency data is shown in this plot with 21814 samples in an hour.

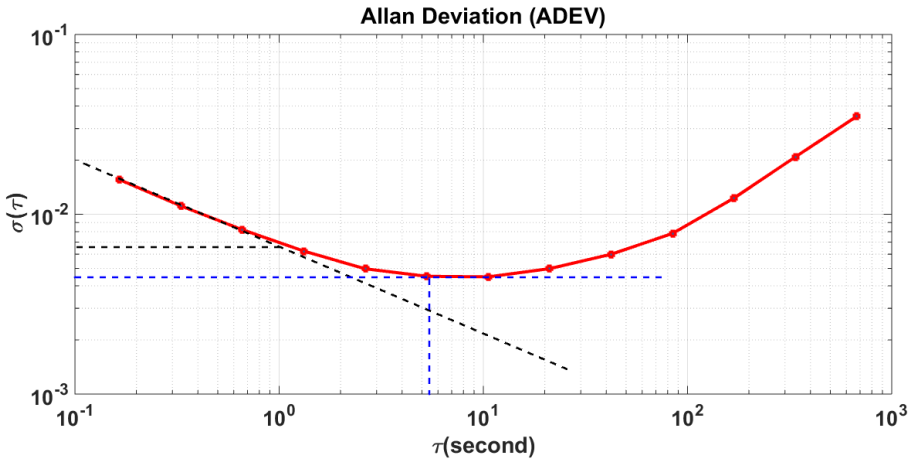


Figure 4.11: Allan deviation plot of the sensor at room temperature.

CHAPTER 5

CONCLUSION AND FUTURE WORKS

5.1 Summary

This thesis mainly focuses on the closed-loop design for a DETF MEMS resonator in XFAB 0.35μm CMOS Process. The goal of the design is to study and characterize the noise and phase noise performances of the closed loop circuit. Thus, the resolution improvement can be accomplished by minimizing the noise in the loop.

In chapter two, characteristics of the resonator, the possible readout topologies and their differences from far-from-carrier phase noise perspective have been studied. The main intention in this chapter is to understand how noise in the open-loop circuitry will behave after closing the loop. To achieve this goal, two different phase noise evaluation methods are discussed. It has been shown that the difference between these two methods is related to the dependency of f^{-1} phase noise component on the signal power. According to [6], f^{-1} phase noise component is not dependent on the signal power while in [3] all the noise sources are scaled up by the signal power at the oscillation frequency. Additionally, it has been shown that the closed-loop circuit with an automatic gain control block has a superior performance from far-from-carrier phase noise point of view. Therefore, as the amplitude limiting technique, AGC is employed in the closed-loop design in CMOS technology.

In chapter three, a closed-loop design with an automatic gain control block is implemented in XFAB 0.35μm CMOS Process based on the models from chapter two. At the beginning of this chapter, minimum possible noise floor is determined as the goal of the design. Then it has been attempted to predict noise behavior of the closed-loop

circuitry by using the noise performance of open-loop circuitry. The minimum noise floor is assumed to be equal to the motional resistance of the resonator. This assumption is made because, at the steady state this amount of resistance is provided by the electronic circuit. -107.6 dBc/Hz is set as the goal of the design and achieved in the simulation results. Since the case study in this thesis is a temperature sensor, the sensor resolution when "white phase" noise is filtered out is calculated to be 0.0219°C. It has been shown in this chapter that the VGA has the dominant effect on the flicker (close-to-carrier or parametric) noise performance of the loop. On the contrary, the input referred voltage noise of the operational amplifier along with the input parasitic capacitance determine the thermal (far-from-carrier or additive) noise performance of the loop.

If a few stages of VGA could be used in the loop to increase the gain range, the gain of trans-resistance amplifier could be increased and consequently better SNR could be achieved. Employing two or three stages of VGA in the loop is limited by the flicker noise performance of the VGA since the implemented VGA in this study owns higher flicker noise PSD. Reducing the flicker noise of the VGA stage can be considered as the future work.

In chapter four, the implemented closed-loop circuit in CMOS technology is built up again with discrete components to evaluate the functionality of the model. For the case when "white phase", "flicker phase" and "white frequency" noise sources are averaged out, Bias instability for this sensor is measured to be 0.0045°C for an averaging time of 5.28 seconds.

Only "white phase" is filtered out in the sensor resolution calculation for the implemented circuit in CMOS Technology. While for the designed circuit with discrete components, the sensor resolution is calculated by doing "white phase", "flicker phase" and "white frequency" averaging. That's one of the reasons why the discrete based circuit design achieves better resolution performance.

5.2 Future Works

There are some issues that can be considered as the future works:

The possible noise contribution of the automatic gain control block is not considered in the closed-loop design, it is possible to evaluate how the AGC block can affect the output noise of the closed-loop circuit in the future. Noise contribution of the MEMS resonator is not evaluated in the closed-loop circuit design as well. It is also desirable to evaluate how nonlinearities from the resonator might affect the close-to-carrier phase noise. Evaluation of the implemented closed-loop circuitry with discrete components is done only by Allan deviation and with a frequency counter. The phase noise measurement setup can be constructed to study the noise performance of the closed-loop circuit much better.

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