DESIGN OF A TUNABLE WIDEBAND BANDPASS FILTER BASED ON SUBSTRATE INTEGRATED WAVEGUIDE TECHNOLOGY FOR CHANNELIZED RECEIVERS

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ABSTRACT

DESIGN OF A TUNABLE WIDEBAND BANDPASS FILTER BASED ON SUBSTRATE INTEGRATED WAVEGUIDE TECHNOLOGY FOR CHANNELIZED RECEIVERS

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In this thesis, a compact-size wideband bandpass filter (BPF) design that can operate in the S/C Band is presented. High out-of-band rejection, low insertion loss, and high return loss are other advantageous features achieved. The proposed BPF is suitable for use in satellite communication, channelized receivers, front-end units, measurement, and test devices. A hybrid approach combining lumped capacitors and the substrate-integrated waveguide technique is chosen to create the BPF. The goal is to decrease the size of BPF while improving its ability to shield it from the outside. The initial stage is constructing the fundamental resonator. A thorough analysis is conducted for the parameters influencing the resonator performance. After that, analytical and computational approaches are used to investigate the dual coupling. Then, a fourth-order BPF design is developed. Moreover, the optimality of the filter is verified using particle swarm optimization. Following that, an electrically tunable version of the filter is enhanced using varactor diodes. The lower and upper cutoff frequencies can be modified separately by employing two distinct voltages transmitted via wire bonds. This layout modification results in a minimal enlargement of the filter and negligible power consumption. Circuit representations of the BPFs and their

correlation with simulations are also investigated to aid and expedite the design process. Finally, ground capacitors are converted into a distributed form for finely tuned capacitance values. Using an iterative grid search process, the ideal parallel plate dimensions for the widest band are determined. All designed BPFs are manufactured and tested.

Keywords: Substrate Integrated Waveguide, Bandpass Filters, Tunable, Channelized Receiver

ÖZ

KANALLI ALMAÇLAR İÇİN ALT TAŞ TÜMLEŞİK DALGA KILAVUZU TEKNOLOJİSİ TEMELLİ AYARLANABİLİR GENİŞ-BANTLI BANT GEÇİREN FİLTRE TASARIMI

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Bu tezde, S/C Bandında çalışabilen kompakt boyutlu bir geniş bantlı bant geçiren filtre (BPF) tasarımı sunulmaktadır. Yüksek bant dışı reddetme, düşük ekleme kaybı ve yüksek geri dönüş kaybı elde edilen diğer avantajlı özelliklerdir. Önerilen BPF uydu iletişiminde, kanallı almaçlarda, ön uç ünitelerde, ölçüm ve test cihazlarında kullanıma uygundur. BPF yi oluşturmak için toplu kapasitörleri ve alt taş tümleşik dalga kılavuzu tekniğini birleştiren hibrit bir yaklaşım seçilmiştir. Amaç, BPF nin boyutunu küçülterek onu dışarıdan koruma yeteneğini geliştirmektir. İlk aşama temel rezonatörün oluşturulmasıdır. Rezonatörün performansını etkileyen parametreler için kapsamlı bir analiz yapılmıştır. Daha sonra ikili bağlantı mekanizmalarını araştırmak için analitik ve hesaplamalı yaklaşımlar kullanılmıştır. Araştırma sonucunda dördüncü dereceden bir BPF tasarımı geliştirilmiştir. Ayrıca, filtrenin eniyiliği parçacık sürüsü optimizasyonu kullanılarak doğrulanmıştır. Bunu takiben, varaktör diyotlar kullanılarak filtrenin elektriksel olarak ayarlanabilen versiyonu geliştirilmiştir. Alt ve üst kesme frekansları, tel bağlar yoluyla iletilen iki farklı voltajın kullanılmasıyla

ayrı ayrı değiştirilebilir. Tasarlanan BPF üretilerek test edilmiştir. Bu tasarım değişikliği, filtrenin minimum düzeyde genişlemesine ve ihmal edilebilir güç tüketimine neden olmuştur. BPFlerin devre gösterimleri ve simülasyonlarla uyumlulukları, tasarım sürecine yardımcı olmak ve hızlandırmak için araştırılmıştır. Son olarak toprak kapasitörleri, ince ayarlı kapasitans değerleri oluşturmak ve eleman sayısını azaltmak için dağıtılmış bir forma dönüştürülmüştür. Yinelemeli bir ızgara arama süreci kullanılarak, en geniş bant aralığı için ideal paralel plaka boyutları belirlenmiştir.

Anahtar Kelimeler: Alt Taş Tümleşik Dalga Kılavuzu, Bant Gerçiren Filtre, Ayarlanabilir, Kanallı Almaç

To my beloved ones...

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TABLE OF CONTENTS

ABSTRACT v

ÖZ vii

ACKNOWLEDGMENTS x

TABLE OF CONTENTS xi

LIST OF TABLES xiv

LIST OF FIGURES xv

LIST OF ABBREVIATIONS xxi

CHAPTERS

1 INTRODUCTION 1

1.1 Motivation and Problem Definition 1

1.2 Brief Review of Literature 5

1.3 Contributions and Novelties 10

1.4 The Outline of the Thesis 11

2 THEORETICAL BACKGROUND OF MICROWAVE FILTERS 13

2.1 Chebyshev Filter Design 14

2.2 Filter Design with Admittance Inverters 18

2.3 Coupling Analysis 21

2.3.1 Electrical Coupling 21

2.3.2 Magnetic Coupling 23
2.3.3 Mixed Coupling 24
2.4 Filters with Substrate Integrated Waveguide 25
3 SIW BANDPASS FILTER DESIGN 31
3.1 Resonator Design 31
3.2 BPF Design Specifications 40
3.3 BPF Design 40
3.4 Coupling Analysis of Designed Filter 44
3.5 Group Delay Analysis of Designed Filter 50
3.6 Simulation Results 51
3.7 Circuit Representation 55
3.8 Particle Swarm Optimization to Verify Filter Optimality 67
3.9 Manufacturing Process 72
3.10 Measurement Setup and Results 75
4 TUNABLE SIW BANDPASS FILTER DESIGN 79
4.1 Tuning Mechanism Determination 79
4.2 Design Procedure 81
4.3 Circuit Representation 86
4.4 Manufacturing and Measurement Results 90
4.5 Optimized Tunable SIW Bandpass Filter with Distributed Ground Capacitances 94
4.6 Manufacturing and Measurement Results 99
5 CONCLUSIONS 103

REFERENCES 107

APPENDICES

A PSO ALGORITHM FUNDAMENTALS 117

B VARACTOR DIODE BASICS 119

C DATASHEET OF VARACTOR DIODE 121

LIST OF TABLES

TABLES

Table 2.1 Table of Element Values 16

Table 3.1 Design Specifications of BPF 40

Table 3.2 Calculated Characteristic Admittance Values 41

Table 3.3 E-Field Measurements of Resonators in BPF 63

Table 3.4 Resultant Values of Improved Circuit Components 64

Table 3.5 Resultant Values of Initial Circuit Components 65

Table 3.6 PSO Parameters 70

Table 4.1 Resultant Values of Circuit Components for Tunable BPF 89

Table 4.2 Resultant Values of Circuit Components for Tunable BPF with Distributed Capacitances 98

LIST OF FIGURES

FIGURES

Figure 1.1 RF Transceiver Block 2

Figure 1.2 Intended Filter Design Location in Superheterodyne Receiver . . 4

Figure 1.3 Electric field in the SIW cavity resonator for different modes (a)full-mode, (b)half-mode, (c) quarter-mode, (d) eight-mode, (e) sixteenth-mode, (f) thirty-second-mode [30] 7

Figure 1.4 Cross section of SIFW 8

Figure 1.5 Cross section of SISW 8

Figure 1.6 Cross section of RSIW 9

Figure 2.1 Filter Response for Different Approaches [59] 14

Figure 2.2 Order Determination of Filter [58] 15

Figure 2.3 Lowpass Filter Prototypes 16

Figure 2.4 Bandpass Filter Transformation Formulas 18

Figure 2.5 Inductance in Inverter Form 19

Figure 2.6 LPF with Inverters 20

Figure 2.7 BPF with Inverters 20

Figure 2.8 Electrical Coupled Circuit [9] 22

Figure 2.9 Equivalent of Electrical Coupled Circuit [9] 22

Figure 2.10 Magnetic Coupled Circuit [9] 23

Figure 2.11 Equivalent of Magnetic Coupled Circuit [9] 23

Figure 2.12 Mixed Coupled Circuit [9] 24

Figure 2.13 Equivalent of Mixed Coupled Circuit [9] 25

Figure 2.14 SIW Structure 26

Figure 2.15 Region of Interest for SIW [60] 27

Figure 2.16 Surface Current for TE_{10} of SIW 27

Figure 3.1 Resonator Structure 32

Figure 3.2 S-Parameters of Resonator with Changing Via Length 33

Figure 3.3 S-Parameters of Resonator with Changing Via Diameter 33

Figure 3.4 S-Parameters of Resonator with Changing Cavity Width 34

Figure 3.5 S-Parameters of Resonator with Changing Patch Width 35

Figure 3.6 S-Parameters of Resonator with Changing Patch Length 35

Figure 3.7 S-Parameters of Resonator with Changing Gap 36

Figure 3.8 Characteristic Impedance Value for Changing Coplanar Waveguide Width 39

Figure 3.9 Designed BPF 42

Figure 3.10 Short Circuit Line Forms in Designed BPF 43

Figure 3.11 Stackup of Designed BPF 44

Figure 3.12 Dual Resonator Design 45

Figure 3.13 Coupling Structures of Dual Resonator Design 46

Figure 3.14 S-Parameters of Externally Uncoupled Resonators with Changing Short Circuit Line Width 47

Figure 3.15 S-Parameters of Externally Uncoupled Resonators with Changing Via Distance 48

Figure 3.16 S-Parameters of Externally Uncoupled Resonators with Changing Electrical Capacitance and Short Circuit Line Layer 49

Figure 3.17 Group delays with Changing External Coupling Capacitance . . 51

Figure 3.18 Simulation Result of Designed Bandpass Filter 52

Figure 3.19 E-Field Distribution of Designed BPF 53

Figure 3.20 H-Field Distribution of Designed BPF 53

Figure 3.21 SIW Cavity Configuration 54

Figure 3.22 S Parameters of SIW Cavity 54

Figure 3.23 E Filed Distribution of SIW Cavity 55

Figure 3.24 Circuit Representation of Bandpass Filter 56

Figure 3.25 Improved Circuit Representation of Bandpass Filter 57

Figure 3.26 Physical Counterparts of Circuit Elements in Improved Circuit Model 58

Figure 3.27 Inductance of Through Via Used in Designed Filter 58

Figure 3.28 Short Circuit Line Pattern in Designed Filter 59

Figure 3.29 Inductance of Short Circuit Line Used in Designed Filter 59

Figure 3.30 Dimension Parameters of BPF Design 60

Figure 3.31 E-Field Measurements for Phase 130° 62

Figure 3.32 S parameters for Short Circuit Line at Lower Layer 65

Figure 3.33 S parameters for Short Circuit Line at Upper Layer 66

Figure 3.34 S parameters for Short Circuit Line at Lower Layer 66

Figure 3.35 S parameters for Short Circuit Line at Upper Layer 67

Figure 3.36 Flow Chart of the Optimization Algorithm for BPF Design . . . 69

Figure 3.37 Inertia Weight Change Over Iterations 70

Figure 3.38 S Parameters of Initial BPF 71

Figure 3.39 Function Value for Each Iteration 71

Figure 3.40 S Parameters of BPF Design for Different Iterations 72

Figure 3.41 SMP Connector 73

Figure 3.42 Layout of Designed BPF 74

Figure 3.43 Manufacturing Result of Designed BPF 74

Figure 3.44 Measurement Setup 75

Figure 3.45 Simulation and Measurement Results of Designed BPF 76

Figure 3.46 S_{21} Parameter Comparison of Measured vs. Simulated with Capacitance Tolerance in the BPF 77

Figure 4.1 Equivalent Circuit of Varactor Diode 80

Figure 4.2 Circuit Design with Varactor Diode 82

Figure 4.3 Manufacturing Outcome of Circuit Design with Varactor 83

Figure 4.4 MA46H120 Performance Curve 83

Figure 4.5 S Parameter of Circuit Design with Varactor 84

Figure 4.6 Second Version of BPF 85

Figure 4.7 S Parameter of Tunable BPF 86

Figure 4.8 Circuit Representation of Tunable Filter 87

Figure 4.9 Physical Equivalents of the Added Circuit Elements in the Filter Design 87

Figure 4.10 Short Circuit Line Structure of Tunable BPF 88

Figure 4.11 Inductance of Short Circuit Line Used in Designed Tunable Filter 88

Figure 4.12 Simulation and Measurement Results of Tunable BPF 90

Figure 4.13 Stackup of BPF v2 91

Figure 4.14 Layout of BPF v2 91

Figure 4.15 Manufacturing Result of Tunable BPF with Lumped C 92

Figure 4.16 Measurement Setup for Tunable Filters 93

Figure 4.17 Measurement Result of Tunable BPF with Lumped Capacitances 93

Figure 4.18 Grid Search Map for the Ground Capacitance Combinations . . . 95

Figure 4.19 Tunable BPF Top View 95

Figure 4.20 Simulation Results of Tunable BPF with Distributed Capacitances for Limit Voltage Values 96

Figure 4.21 Simulation Results of Tunable BPF with Distributed Capacitances for Higher Cutoff Tuning 96

Figure 4.22 Simulation Results of Tunable BPF with Distributed Capacitances for Lower Cutoff Tuning 97

Figure 4.23 Simulation and Measurement Results of Tunable BPF with Distributed Capacitances 98

Figure 4.24 Stackup of Tunable BPF with Distributed Capacitances 99

Figure 4.25 Final Version of Layout 100

Figure 4.26 Intermediate Layer of Layout 100

Figure 4.27 Manufacturing Result of Tunable BPF with Distributed C 101

Figure 4.28 Frequency Response of Tunable BPF with Distributed Capacitances for Lower Cutoff Tuning 102

Figure 4.29 Frequency Response of Tunable BPF with Distributed Capacitances for Higher Cutoff Tuning 102

Figure A.1 Three common scenarios for the particles in PSO processes (a) Starting phase (b) Middle phase (c) Final phase [46] 117

Figure B.1 Varactor Diode Structure 119

Figure B.2 Forward Biased Varactor 120

Figure B.3 Reverse Biased Varactor 120

LIST OF ABBREVIATIONS

ACO	Ant Colony Optimization
ADC	Analog-to-Digital Converter
BW	Bandwidth
CAD	Computer-Aided Design
DE	Differential Evolution
EM	Electromagnetic
ESR	Equivalent Series Resistance
FBW	Fractional Bandwidth
GA	Genetic Algorithms
HFSS	High Frequency Structure Simulator
HMSIW	Half-Mode Substrate Integrated Waveguide
IL	Insertion Loss
LNA	Low Noise Amplifier
MEMS	Micro-Electromechanical System
PCB	Printed Circuit Board
PSO	Particle Swarm Optimization
QMSIW	Quarter-Mode Substrate Integrated Waveguide
RF	Radio Frequency
RSIW	Ridge Substrate Integrated Waveguide
RWG	Rectangular Waveguide
RZ	Reflection Zero
SIFW	Substrate Integrated Folded Waveguide
SISW	Substrate Integrated Slab Waveguide
SIW	Substrate Integrated Waveguide

SMP	SubMiniature Push-on
SNR	Signal-to-Noise Ratio
TE	Transverse-Electric
TM	Transverse-Magnetic
TZ	Transmission Zero
VNA	Vector Network Analyzer

CHAPTER 1

INTRODUCTION

1.1 Motivation and Problem Definition

Radar and communication technologies have been an indispensable part of modern life for the past century. As technology advances, people demand to transmit data with higher data rates to increase the speed of communication, lower power consumption for efficient transmission, and larger bandwidth (BW) for the ability to transmit more information. As a result, people started investigating higher frequencies known as microwave frequencies for applications [1].

Different types of microwave components have been developed in order to be used at these frequencies, and they have been combined to form functional circuits and systems. Some of these essential microwave components are power dividers, filters, couplers, isolators, limiters, and circulators. Specifically, filters are being utilized in these systems on both the receiver and transmitter side to select the desired frequency with desired BW and mitigate spurious signals, harmonics of fundamental signals, and any other unwanted signals sourced from system elements [2]. Figure 1.1 illustrates the locations where filters are placed to achieve these objectives in a typical transceiver block. Filter performance is expected to increase with the complexity of communication operations on technologies [3]. There are a couple of challenges that should be overcome during the design of the filter.

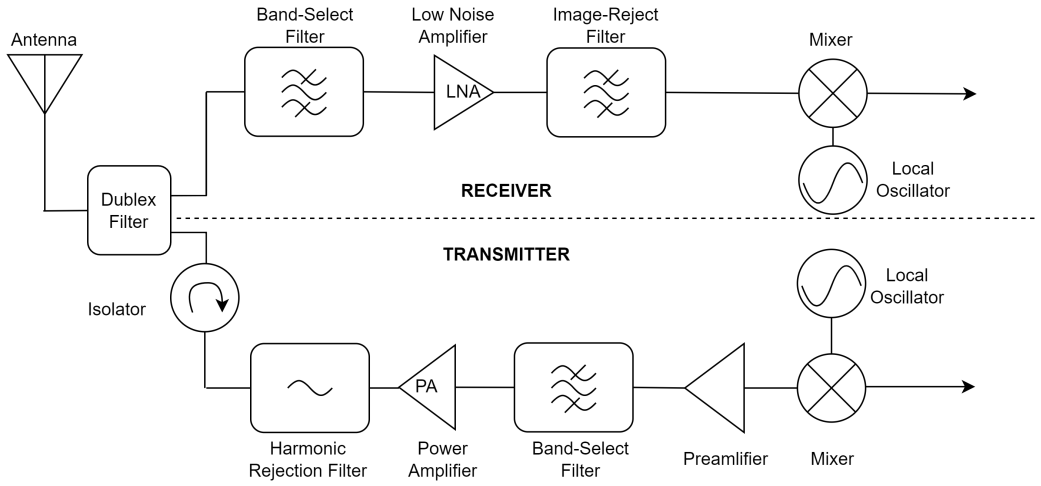


Figure 1.1: RF Transceiver Block

The first one is that the composed filter should have low insertion loss (IL) with desired frequency selectivity so that the receiver of the system has a good noise figure. At microwave frequencies, filters tend to have more IL compared to lower frequencies because of increasing material losses, radiation losses, parasitic effects, etc. Hence, keeping a balance between low IL and good frequency selectivity is a challenge.

The second challenge is constructing a compact filter for the desired frequencies. Maintaining filter performance while achieving a small footprint is difficult since it reduces the amount of space that can be used for filter components.

Another challenge is that radio frequency (RF) filter performance can be significantly impacted by slight changes in material characteristics, dimensions, or manufacturing techniques. Because of that, manufacturing tolerances should be considered and compensated during the design process.

One such obstacle to be addressed is lowering the cost of manufacturing the intended filter. Depending on the method employed, the choice of the materials and their suitability for high-volume manufacturing may reduce the manufacturing costs.

In field applications, it could be necessary to make minor adjustments to the characteristics of the filter to help the system adjust to changing conditions faster. Depending on the situation, it may be desirable to change the lower or higher cutoff frequency values individually or in parallel. Nonetheless, these adjustments must be made ex-

peditiously and practically so as not to significantly impair the functionality of the filter.

Finally, there has always been a trade-off between the previously mentioned qualities. If one needs a filter with a compact size, some of the specifications such as low loss or good power handling should be loosened. Thus, the design technique should be chosen appropriately for implementation.

If the structure used in this study is examined in detail, the superheterodyne receiver structure should be focused on. The purpose of this receiver, which can be used in radar, communication, measurement, or test systems, is to capture the signal transmitted in the air, amplify the weakened signal, and purify it from unwanted signals. After that, receivers multiply the targeted signal they receive with various frequencies with the help of a mixer to convert it into a usable frequency band. In this way, the frequency is converted to a higher or lower frequency value depending on the application and becomes suitable for signal processing. The RF strip in the receiver includes a filter bank to suppress unwanted signals. The filter bank provides the possibility of detailed analysis of incoming signals by dividing a wide frequency spectrum into several channels. Since only the signal element in the relevant channel is passed and those in other bands are suppressed, the selectivity of the receiver increases and unnecessary broadband processing load is eliminated. Using a filter also has the benefit of removing strong out-of-band signals that are undesirable, which permits the low noise amplifier (LNA) to function linearly without leading compression. This increases the dynamic range, or in other words the range between the lowest to the highest signal strength that the receiver can detect without distortion. Because of this, even if it slightly increases the noise figure before LNA, its low IL and enhanced dynamic range justify its employment. Additionally, being able to select different channels increases the flexibility of the receiver and makes it easier to adapt to different user requirements.

This study aims to design a filter to be used in one channel of the channelized receiver as shown in Figure 1.2. For this reason, the BW and center frequency that the filter should have are selected specifically for the application. A high attenuation level of the filter at certain out-of-band frequencies is crucial. This prevents the system

from receiving undesired off-channel signals, such as jamming signals, ambient noise, spurious emissions, or interference from other systems or the transmitter within its system. Keeping the size of the design within the bounds of the previously utilized filter is another important goal. This means that the filter should be realized in an area smaller than $0.175\ \lambda \times 0.68\ \lambda$ where λ is the wavelength of the center frequency. In fact, the design must be as compact and easy to manufacture as possible given that it is anticipated to be used extensively. Moreover, a high return loss is required when offering previously mentioned functions in order to minimize signal reflections and avoid mismatch. Furthermore, to preserve a high signal-to-noise ratio (SNR) and prevent a critical decrease in signal power, there should be minimal IL.

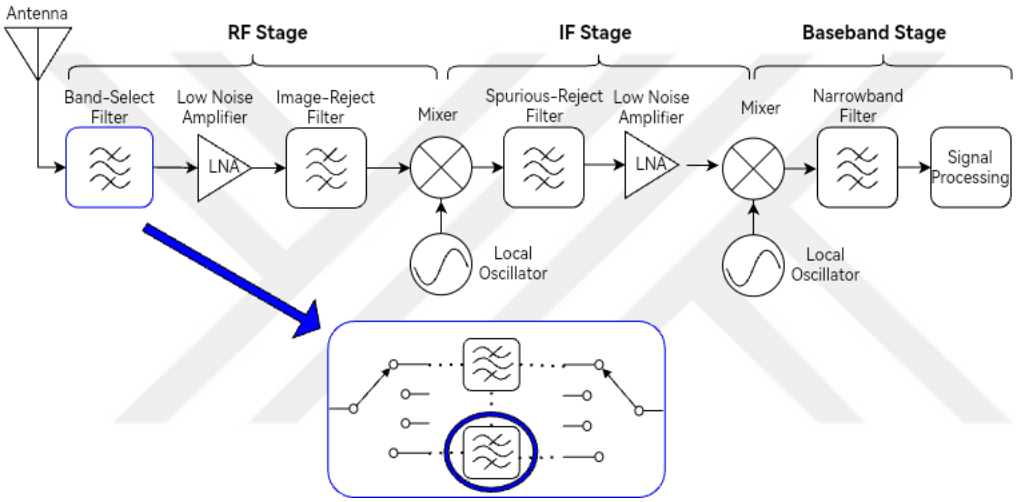


Figure 1.2: Intended Filter Design Location in Superheterodyne Receiver

There are several reasons why the RF domain is used when constructing filters, even though filters with better specifications can be developed in the digital domain. The first of these is that an analog filter is used in the receiver structure where the filter is intended to be used. Considering that this structure has been modified and the direct sampling method has been chosen, the analog-to-digital converter (ADC) for direct sampling must sample the wide frequency band at a high sample rate [4]. This requires an undesirably high amount of power and time to complete processing. The second reason is that even in systems with direct sampling, analog filtering is performed before the ADC to prevent aliasing and to ensure that the ADC operates within its own linear range [5]. On the other hand, in order to use digital filters, the signal must be converted to the digital domain with an ADC.

To sum up, compact design, low manufacturing costs, low IL, and high-frequency selectivity are required, in addition to better quality factors. Also, manufacturing tolerances and other system integration factors should be suitable for a user-friendly filter. Thus, a tunable Substrate Integrated Waveguide (SIW) bandpass filter with better qualifications for the usage of radar transmitters and receivers is aimed to be designed in the thesis.

1.2 Brief Review of Literature

It is essential to comprehend where the tunable semi-lumped SIW bandpass filter, which is intended to be designed in this work, currently stands in the literature and what contribution it provides. Researchers have used a wide range of methodologies to conduct filter designs from the past to the present.

The inter-digital filter is one of these methods, and it has been used in numerous research [6–8]. For example, an interdigital filter with a 6 GHz center frequency with a fractional BW of 29.92% is designed in the study [6]. Moreover, the dimensions of the filter are $0.35\ \lambda \times 0.14\ \lambda$. The method uses coupling between two parallel RF lines to construct filter characteristics. Even though the method provides very small and low-loss designs, particularly for low frequencies, the quality factor decreases as the frequency increases. At this point, a hybrid solution with SIW design offers a high-quality factor and minimal loss, resulting in a compact design.

The second technical example is microstrip filters. Studies in [9–11] are some of the example studies. For instance, in the study [11], a wideband microstrip filter with a center frequency of 4 GHz, and dimensions of $0.27\ \lambda \times 0.17\ \lambda$ is designed. These are filters obtained by using planar transmission lines in various ways. Like the previous technique, it has a compact and easily manufactured structure. However, unlike hybrid SIW, a more careful design is required to prevent the amount of loss from increasing as the frequency increases.

Cavity and waveguide filters are other alternative techniques [12–15]. In the former method, the filter response is created by using resonant cavities, and in the latter method, by using metallic waveguides in the form of different geometries. Both

techniques have very low losses and high-quality factors with great power-handling capabilities. Nevertheless, these structures are large, heavy, and difficult to use with planar designs. Also, high manufacturing costs make them less profitable to use. For example, in the study [13], a four-pole cavity filter with a fractional bandwidth of 13% and a center frequency of 3.9 GHz is designed. The filter has dimensions of 0.46 $\lambda \times$ 0.18 λ and an IL of 0.14 dB. The designed structure in this study can be integrated into planar structures more easily and is lightweight [16].

As the fourth subject, lumped element filter studies can be examined [17, 18]. A highly compact dual-band lumped-element bandpass filter with passbands at 2.4 and 5.2 GHz is illustrated with approximately 20% fractional BW as an example in [17]. Although these designs are advantageous to use at low frequencies, they have limited performance compared to SIW designs as the frequency increases. In addition, the fact that there are only lumped elements at certain values is a factor that makes the design difficult. Parasitic effects and resistive loss in the components increase, and the quality factor lowers with increasing frequency. Furthermore, usage becomes challenging as frequency increases since the element size gets considerably smaller than the appropriate size. For these reasons, semi-lumped SIW is likely to be preferred for high frequency compared to the lumped-only technique.

If one wants to examine the SIW technique in more detail, the SIW technique was first proposed in 2001 [19]. Then, SIW structures started to be utilized extensively in radar and communication system designs because of their many advantages over planar and waveguide structures [19, 20]. A wide range of active and passive RF elements have been developed with the SIW and are currently widely used [21–26]. Filters are one of those elements designed using the SIW technique. Studies have been carried out to improve RF filters designed using SIW topology, focusing on many different features.

The first feature frequently studied in articles is the miniaturization of the SIW filter. Various configurations and application approaches have been suggested to enable the developed SIW filters to remain technologically advanced while fitting into smaller spaces. One of them involves altering the field path without altering the operating mode which passes through the filter by substituting real structure with the symmetry plane i.e., a virtual magnetic wall is created. Half-mode SIW (HMSIW) [27], and

quarter-mode SIW (QMSIW) [28, 29] are some examples of these. The distribution of the electric field in the SIW cavity resonator for different SIW modes is depicted in Figure 1.3. As can be understood from Figure 1.3 and the conducted studies, while the size is reduced by half in HMSIW, QMSIW provides a reduction of a quarter size without changing the field distribution. Further reduction is also possible with the utilization of other SIW mode topologies. On the other hand, the use of this model in structures such as filters may cause electromagnetic (EM) leakage, since the shielding on one side is removed [30].

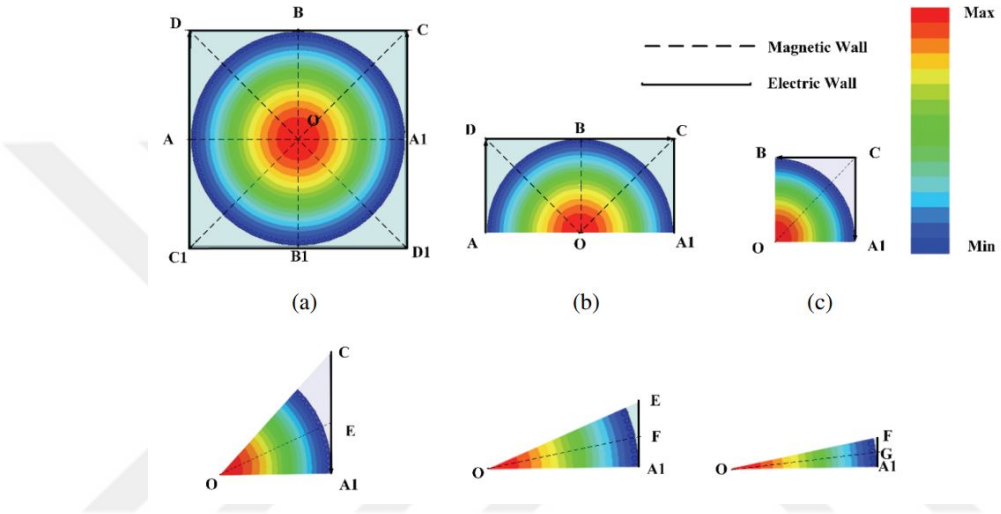


Figure 1.3: Electric field in the SIW cavity resonator for different modes (a)full-mode, (b)half-mode, (c) quarter-mode, (d) eight-mode, (e) sixteenth-mode, (f) thirty-second-mode [30]

Another technique for nearly halving the size of the filter design is the folded structure method. Many studies have been conducted on substrate-integrated folded waveguide (SIFW) in the literature [31–33]. Figure 1.4 shows a cross-section of a basic SIFW structure [34]. By increasing the layer number in the printed circuit board (PCB), the number of folds can also be increased. This results in a decrease in the width of the design at the same rate. However, the disadvantage of the SIFW method is that it has a more complex manufacturing process than the previous method because of the multi-layer design.

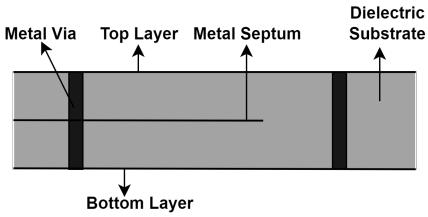


Figure 1.4: Cross section of SIFW

The substrate-integrated slab waveguide (SISW) is an alternative solution that aims to locally change the effective dielectric permittivity value on the PCB by opening air holes in the PCB. In this way, the cutoff frequency of the second mode is increased to reduce the size of the filters [35, 36]. Equation (2.38) whose theoretical basis is provided in Chapter 2, validates this relationship. A cross-section of a simple SISW structure is shown in Figure 1.5.

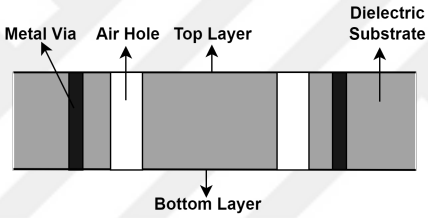


Figure 1.5: Cross section of SISW

Ridge SIW (RSIW) is another method that has been suggested to reduce the size of the filter. This structure is constructed utilizing a partially installed via row in the middle and is modeled based on the ridge structure of the waveguide. Since the same cutoff frequency can be achieved with smaller sizes using RSIW, the targeted minimization goal has been achieved [37]. The RSIW structure cross-section is depicted in Figure 1.6.

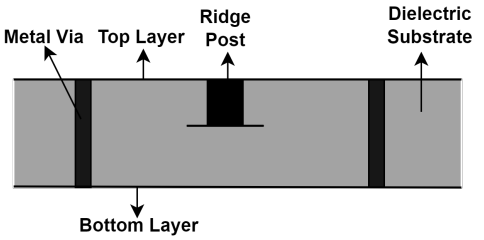


Figure 1.6: Cross section of RSIW

Even though all the aforementioned techniques significantly reduce the size of SIW filters, alternative methods remain necessary because the dimensions of the filters are still greater than those of microstrip structures. The intended size reduction is achieved when a semi-lumped SIW filter is designed as in [38] and in this study.

Making filters tunable is the second feature that scientists are concentrating on. There are several ways to provide a filter the ability to be adjusted. A few of these may be classified as mechanical, magnetic, or electrical mechanisms [39]. The research that has been done thus far has led to the identification of some benefits and drawbacks for each approach. While mechanical tuning has the drawback of requiring larger and slower mechanisms, it has been discovered that having high power resistance and quality factors are beneficial features [40–42]. More recent research has focused on the subject of electrically reconfigurable filters. It has a rapid tuning mechanism and small dimensions. RF Micro-Electro-Mechanical System (MEMS) switches, variable capacitors, and diodes are some of the elements used for this method [43, 44]. Also, studies have begun to be conducted on electrical tunability in SIW filters as in this study. A broad tuning range is desired while maintaining performance in terms of IL, BW, and out-of-band rejection [44, 45].

Achieving the optimal frequency response by adjusting the values of the filter components is another important consideration throughout the filter design process. It is also aimed to reduce the amount of time lost in determining the best solution to this challenging issue. Several algorithms have been developed by researchers to accomplish this goal [46–49]. However, the algorithms proposed so far do not guarantee whether the outcome they obtain is a local optimal solution or a global optimum solution in the large existing solution set while the design parameters remain within the predeter-

mined bounds. Nevertheless, when it comes to model performance for exploring solution space efficiently, meta-heuristic algorithms rank among the best [50]. Differential Evolution (DE), Genetic Algorithms (GA), Particle Swarm Optimization (PSO), and Ant Colony Optimization (ACO) can be given as examples of metaheuristic algorithms. The evolutionary algorithm to be used is selected in the studies according to the characteristics of the problem and solution set. The features and differences of these algorithms are shown in the study [51]. For reasons such as its speed, simplicity of implementation, and suitability for continuous models, the PSO algorithm has been employed in numerous filter optimization studies like in this study [46, 50, 52, 53].

1.3 Contributions and Novelties

The main contributions of this thesis are as follows:

- A hybrid bandpass SIW filter with a compact size existing in the literature is modified to fit the intended frequency band and its design parameters are adjusted to fit the workflow of the intended manufacturing system.
- A new lumped circuit model is developed that better matches the frequency response of the filter than that presented in the referenced work. This topology is explained and its performance is compared with the previously proposed circuit. This newly developed circuit makes it possible to design filters more quickly and systematically.
- PSO is used to create an algorithm that expedites the filter design process. With the aid of the code, the user can quickly determine the ideal lumped capacitance values for this structure by providing initial values.
- The designed filter is upgraded to an electrically tunable version utilizing the varactor diode configuration. The feeding structure suitable for varactors is designed using the wire bond technique. In this way, both high and low cutoff frequencies of the filter can be tuned continuously in a wide range without the need to change elements manually. Furthermore, the power consumed to tune with this method is sufficiently low.

- Ground capacitors of the designed filter are converted to a distributed form in order to reduce the number of elements used in the filter. Another advantage is that while capacitors can take certain values when used as lumped elements, they can be generated in a distributed form with the necessary size. This allows performing fine-tuning in frequency response. In addition, the proportionally large tolerance for lumped capacitors at small capacitance values is minimized in the distributed version. The repeatability and reliability of the filter response are improved in this way.
- The optimal size of the capacitance planes in the distributed form is discovered for a broad frequency range with the aid of the grid search method.
- The circuit representation for the improved adjustable version is studied.

1.4 The Outline of the Thesis

The following explanation applies to each section of the thesis:

Chapter 2 describes the theoretical foundation required for SIW filter design. Filter theory and SIW structures are covered in great detail. Factors affecting filter performance are explained, and the standards used to assess filter performance are stated.

Chapter 3 explains the procedures for designing the filter with the necessary characteristics and performance, based on the information in Chapter 2. The filter is analyzed at each step using various computer-aided design (CAD) tools. EM analysis is conducted using the High-Frequency Structure Simulator (HFSS) [54]. The lumped element circuit representation of the filter is obtained and analyzed using the Genesys software tool. The design parameters are verified in MATLAB [55], where a Particle Swarm Optimization (PSO) algorithm is implemented for optimization. Mentor PADS is used for the PCB layout composition [56]. The outcomes of the simulations are discussed, and the research done to standardize the manufacturing process is highlighted. The chapter concludes with an analysis and comparison of the measured filter performance with the design simulations.

Chapter 4 explains the process of converting the design from the previous chapter into an electrically configurable filter. The chapter begins by exploring tunable configurations. Next, the basics of the varactor diode, which is used to make the filter electrically tunable, are explained. The integration of these diodes into the filter design is then discussed in detail. The simulation results of the design are assessed, and the considerations for making it suitable for manufacturing are described. Q3D and analytical methods are used to extract the circuit representation of the filter from its distributed form [57]. The manufacturing outcome is then examined. Following that, the methodology for converting ground capacitors to distributed form is explained. Finally, the grid search method is used to determine the optimal size of the capacitance planes to achieve the best return loss values across the frequency ranges covered by the tunable filter.

In Chapter 5, the work done throughout the thesis is summarized, evaluated, and concluded. Contributions made through filter design are explained. Finally, future studies that are planned to be carried out are mentioned.

CHAPTER 2

THEORETICAL BACKGROUND OF MICROWAVE FILTERS

It's important to comprehend the function and significance of filters in microwave communication technology. Systems employ filters to attenuate unwanted frequencies while allowing the target frequency band to pass. Based on the passband properties of the filters, they can be divided into four primary categories. These filters are categorized as bandpass, low pass, high pass, and bandstop. Alternatively, they can be divided into three primary categories based on the BWs of filters. Narrowband, wideband, and moderately wideband filters are ways to categorize them. The complexity of communication technology operations raises expectations for filter performance. It is desired to have qualifications such as a higher quality factor with excellent frequency selectivity, low manufacturing costs, and a compact design.

The designer can use a variety of ways to design filters. The first approach uses periodic structures to create filter designs. As the name suggests, a determined structure is placed multiple times to form the desired passband or stopband characteristic [58]. Another concept similar to the periodicity concept is the image parameter method. In a 2-port network, L and T sections which can be calculated using image impedances are repeated to obtain the filter with the desired response. By definition, when one of the ports is terminated with its input impedance, the impedance value observed from the other port is known as the image impedance [58]. The third method is the IL method. While the second method cannot be adjusted to any desired frequency, this method has more flexible solutions in this regard. It is also more practically applicable than the first and second methods. The fact that this design process is more complicated is a drawback. Given the specifications, the designer must select the best IL method from the available options. For example, Maximally Flat, also

known as Binomial or Butterworth filter, is the technique with the flattest passband characteristic. Nevertheless, since the stopband transition is slower, its selectivity is less. Conversely, greater selectivity is achieved with Chebyshev (also known as equal-ripple) filters, but the filter response exhibits ripples in the passband or stopband. Elliptic (Cauer) filters are the most selective alternative, but they have ripples in both the passband and the stopband, and the design method is more complex. Finally, filters created with the linear phase (Bessel) method, prevent distortion in the signal because they have minimal phase change. The disadvantage of using it is that less attenuation is obtained in the stopband, which causes the need to create higher-order filters, and out-of-band suppression is low [58]. The filter response produced by the four previously discussed approaches is summarized in Figure 2.1 [59].

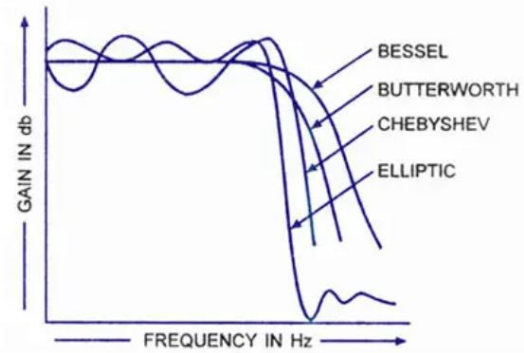


Figure 2.1: Filter Response for Different Approaches [59]

2.1 Chebyshev Filter Design

To create a filter with good out-of-band suppression and a tolerable ripple level because of the design limitations that will be discussed in Section 3.1.3 of this thesis, the Chebyshev IL approach is utilized.

When designing a Chebyshev filter, the design criteria of the target filter are established based on its intended application and role. Some of these design specifications are the cutoff frequency, the determined ripple level in dB, how much attenuation is desired at which frequency, and the source resistance value. Then, using this data, the filter order can be calculated with the help of the formula provided in Equation

(2.1), where n is the order of the filter and ω_c is the cutoff frequency. The desired attenuation A in dB scale is given for the frequency ω_s. In addition, ϵ is the ripple factor that can be calculated using Equation (2.2). r_p is the passband ripple in dB [9].

$$n \geq \frac{cosh^{-1}\left(\sqrt{\frac{10^{A/10}-1}{\epsilon^2}}\right)}{cosh^{-1}\left(\omega_s/\omega_c\right)} \tag{2.1}$$

$$\epsilon = \sqrt{10^{r_p/10} - 1} \tag{2.2}$$

The order determination can be done not only with an equation but also with the help of plots grouped according to ripple level. Attenuation versus normalized frequency curves for equal-ripple filter prototypes with a ripple level (r_p) of 0.5 dB is shown in Figure 2.2 [58].

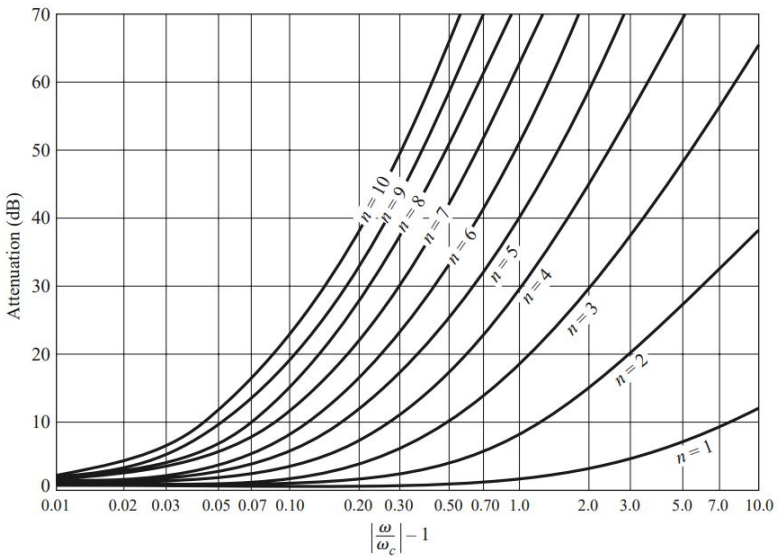


Figure 2.2: Order Determination of Filter [58]

The transfer function of the Chebyshev filter is as in Equation (2.3). The value of the Chebyshev polynomial T_n in the formula changes when the filter order n changes, as seen in Equation (2.4).

$$|S_{21}(w)|^2 = \frac{1}{1 + \epsilon^2 T_n^2(w/w_c)} \tag{2.3}$$

$$T_n(0) = \begin{cases} 0 & \text{for n odd} \\ 1 & \text{for n even} \end{cases} \tag{2.4}$$

After deciding on the order of the filter, finding the values of the components of the low-pass prototype circuit is necessary. For this purpose, tables designed for various ripple levels can be utilized. For instance, Table 2.1 provides element values for 1rad/sec ω_c and 0.5 dB r_p. g_0 has a value of 1, which is not displayed in the Table [58].

Table 2.1: Table of Element Values

n	g_1	g_2	g_3	g_4	g_5	g_6	g_7	g_8	g_9	g_{10}	g_{11}
1	0.6986	1.0000									
2	1.4029	0.7071	1.9841								
3	1.5963	1.0967	1.5963	1.0000							
4	1.6703	1.1926	2.3661	0.8419	1.9841						
5	1.7058	1.2296	2.5408	1.2296	1.7058	1.0000					
6	1.7254	1.2479	2.6064	1.3137	2.4758	0.8696	1.9841				
7	1.7372	1.2583	2.6381	1.3444	2.6381	1.2583	1.7372	1.0000			
8	1.7451	1.2647	2.6564	1.3590	2.6964	1.3389	2.5093	0.8796	1.9841		
9	1.7504	1.2690	2.6678	1.3673	2.7239	1.3673	2.6678	1.2690	1.7504	1.0000	
10	1.7543	1.2721	2.6754	1.3725	2.7392	1.3806	2.7231	1.3485	2.5239	0.8842	1.9841

Figure 2.3 depicts potential lowpass prototype configurations. The image illustrates that the design can begin with a parallel or series element, and the number of elements depends on the degree of the filter.

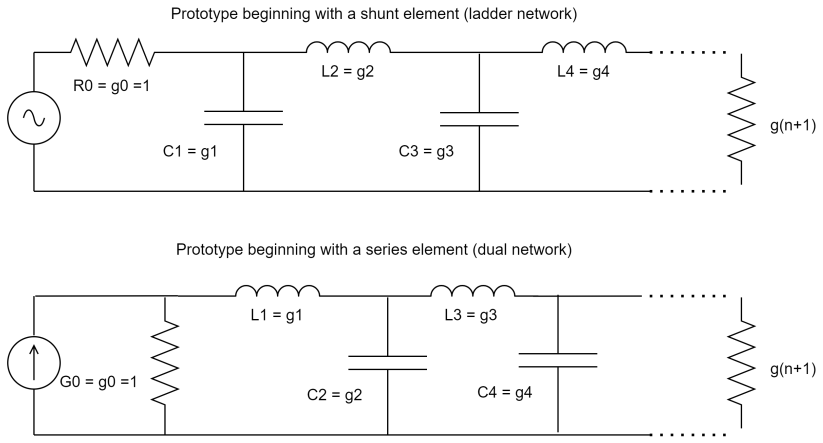


Figure 2.3: Lowpass Filter Prototypes

After selecting the desired configuration for the lowpass prototype, impedance and frequency scaling operations must be performed for element values. The formulas given in Equations (2.5), (2.6), and (2.7) can be used depending on whether the value to be scaled corresponds to inductance, capacitance, or impedance in the configuration. It is significant to remember that g_{n+1} reflects the load conductance in an even order filter and the load resistance in an odd order filter. Therefore, when scaling to determine the load impedance value, the relevant formula in Equation (2.8) should be applied [58].

$$L_n = \frac{g_n R_0}{\omega_c} \tag{2.5}$$

$$C_n = \frac{g_n}{R_0 \omega_c} \tag{2.6}$$

$$R_S = g_0 R_0 \tag{2.7}$$

$$R_L = \begin{cases} g_{n+1} R_0 & \text{for n odd} \\ \frac{R_0}{g_{n+1}} & \text{for n even} \end{cases} \tag{2.8}$$

The same lowpass prototype can be used to create a filter with bandpass characteristics by altering the frequency mapping while leaving the impedance scaling unchanged. The necessary new transformation formulas are displayed in Figure 2.4. Equation (2.9) expresses the computation of the center frequency (ω_0) term utilized in the transformation calculation, given that ω_1 and ω_2 are edge frequencies of the passband. In addition, Equation (2.10) can be used to determine the fractional bandwidth (FBW) (i.e., Δ value) [58].

$$\omega_0 = \sqrt{\omega_1 \omega_2} \tag{2.9}$$

$$\Delta = \frac{\omega_2 - \omega_1}{\omega_0} \tag{2.10}$$

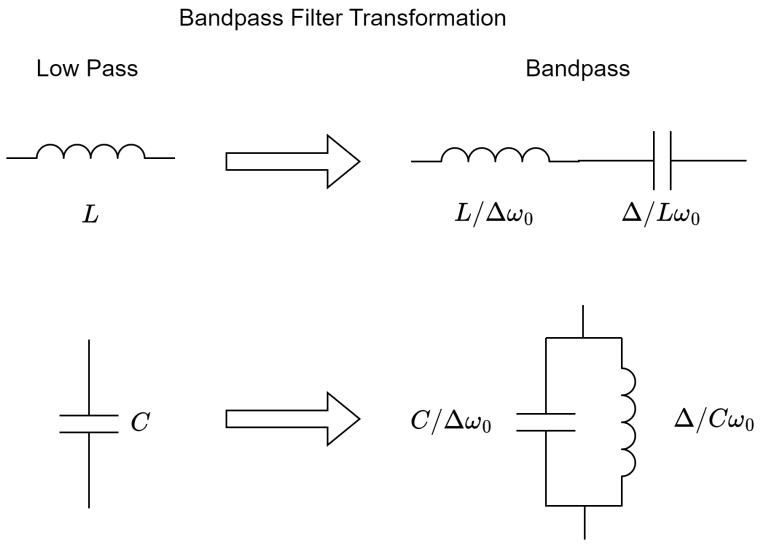


Figure 2.4: Bandpass Filter Transformation Formulas

After conversion to a bandpass filter, each parallel or series-connected LC circuit forms a resonator structure. These resonators are the building blocks for BPF. The frequencies that the filter passes or not are determined by these structures.

2.2 Filter Design with Admittance Inverters

In practical applications, there are certain drawbacks to employing the lumped filter directly from Section 2.1. Despite the practicality of the design, finding lumped components with precise values that provide the required BW and center frequency is challenging. Additionally, as the frequency increases, it becomes more difficult for the design to be completely lumped. The first reason for this is that the component starts to deviate from its intended behavior as a result of an increase in the skin effect and parasitic effect. Consequently, the resistive loss of the components increases and the quality factor decreases. Another reason is that the size of components especially inductors increases to the point where it becomes impractical. Additionally, the distributed character of the signal increases as the signal wavelength becomes more comparable to the physical dimensions of the circuit elements with increasing frequency. On the other hand, with inverters, coupling amount and impedance matching between resonators can be readily achieved without requiring any alterations to the structure

of the resonators. Therefore, BW and center frequency adjustments become more precise with this technique. Although it is not as easy to design as lumped topology, more compact and optimized designs in every aspect can be achieved. Moreover, it can be used at high frequencies and exhibits less loss while allowing for sharper band transitions. These factors make it more advantageous for the designer to utilize the inverter topology in the high-frequency filter than the lumped element.

It is possible to analyze inverters into two categories: impedance and admittance inverters. Since admittance inverters are used in this study, the subject is explained through it. However, the same relationships can be used for impedance inverters. The purpose of using this structure is to shift the admittance value (Y_2) of one port in a two-port network concerning the characteristic admittance (J) value of the inverter. The admittance value observed from the other port is Y_1. Equation (2.11) expresses this relation [58].

$$Y_1 = \frac{J^2}{Y_2} \tag{2.11}$$

A 90-degree phase shift can be achieved because of this configuration. As an outcome, a parallel capacitance connected to port two is perceived as a serial inductance from the first port. Likewise, a series inductance shows a parallel capacitance characteristic when it is examined after the inverter as in Figure 2.5. The ABCD matrix of an ideal inverter is as in Equation (2.12) [9].

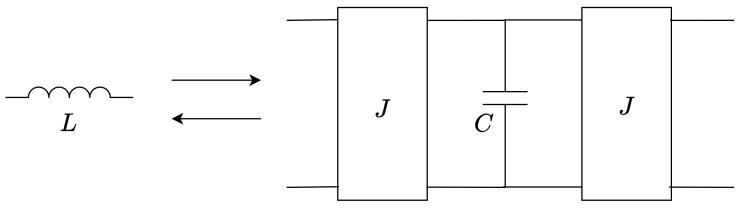


Figure 2.5: Inductance in Inverter Form

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 0 & \pm\frac{1}{jJ} \\ \mp jJ & 0 \end{bmatrix} \tag{2.12}$$

A ladder-form Chebyshev low-pass prototype can be simplified and more manageable by utilizing the impedance conversion capability of the inverter. As can be seen in Figure 2.6, this version requires only inductors or only capacitors. Related formulas for the construction of the filter are Equations (2.13), (2.14), and (2.15) [9].

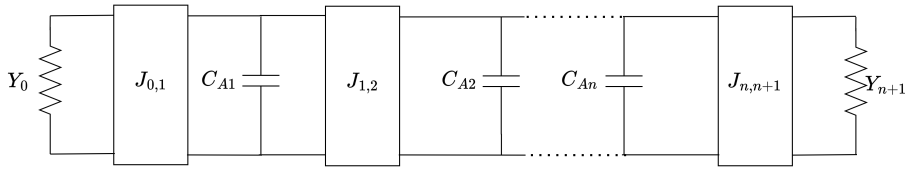


Figure 2.6: LPF with Inverters

$$J_{0,1} = \sqrt{\frac{Y_0 C_{A1}}{g_0 g_1}} \tag{2.13}$$

$$J_{i,i+1} = \sqrt{\frac{C_{Ai} C_{A(i+1)}}{g_i g_{i+1}}} \quad \text{for } 1 < i < n-1 \tag{2.14}$$

$$J_{n,n+1} = \sqrt{\frac{C_{An} Y_{n+1}}{g_n g_{n+1}}} \tag{2.15}$$

Last of all, Figure 2.7 shows admittance inverters integrated into the Chebyshev BPF topology. The J calculation of the first inverter is calculated by Equation (2.16), and the J value of the last inverter is calculated by Equation (2.18). The J values for each intermediate inverter are determined using the formula in Equation (2.17) [9].

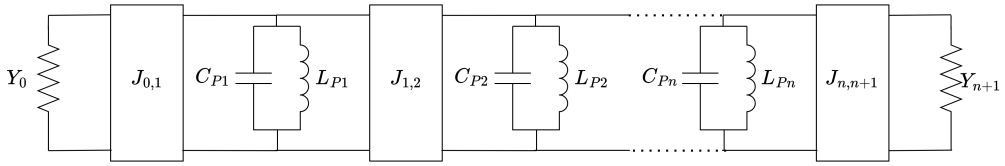


Figure 2.7: BPF with Inverters

$$J_{0,1} = \sqrt{\frac{Y_0 \Delta\omega_0 C_{P1}}{g_0 g_1}} \tag{2.16}$$

$$J_{i,i+1} = \Delta\omega_0 \sqrt{\frac{C_{Pi} C_{P(i+1)}}{g_i g_{i+1}}} \quad \text{for } 1 < i < n-1 \tag{2.17}$$

$$J_{n,n+1} = \sqrt{\frac{\Delta\omega_0 C_{Pn} Y_{n+1}}{g_n g_{n+1}}} \tag{2.18}$$

$$L_{Pi} = \frac{1}{\omega_0^2 C_{Pi}} \quad \text{for } 1 < i < n \tag{2.19}$$

2.3 Coupling Analysis

There are various ways to integrate admittance inverters into filters. However, the common feature of all techniques is to add structures that create impedance transformation and coupling between the resonators. The process of coupling analysis involves analyzing how this additional coupling mechanism behaves concerning different structural variables. Using choices that are appropriate based on the findings of the analysis, the desired coupling coefficient can be obtained. The coupling coefficient is a constant that indicates the coupling strength of the structure added to the filter. The term "synchronously tuned" refers to an analysis where the resonators are the same, as in filters, oscillators, etc.; "asynchronously tuned" refers to an analysis where the resonators are different, as in sensors, optical systems, etc. In this thesis, synchronously tuned resonators are preferred because of reasons such as design practicality, high coupling efficiency, and strength.

2.3.1 Electrical Coupling

Electrical coupling is the term for a phenomenon that happens when two resonators interact via an electric field. Figure 2.8 depicts the circuit of a pair of synchronously tuned electrically coupled resonators, where mutual capacitance C_m is used to represent coupling. The same circuit can also be created with the coupling effect provided by an admittance inverter as in Figure 2.9. In order to conduct even and odd mode analysis in the circuit, symmetrical corrections are made to the C_m capacitance [9].

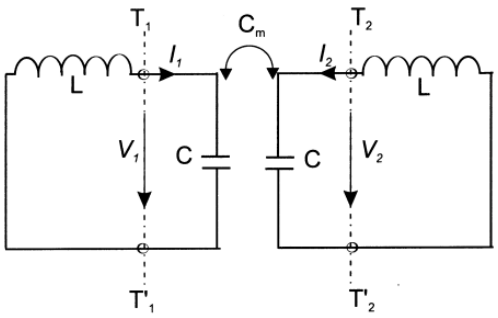


Figure 2.8: Electrical Coupled Circuit [9]

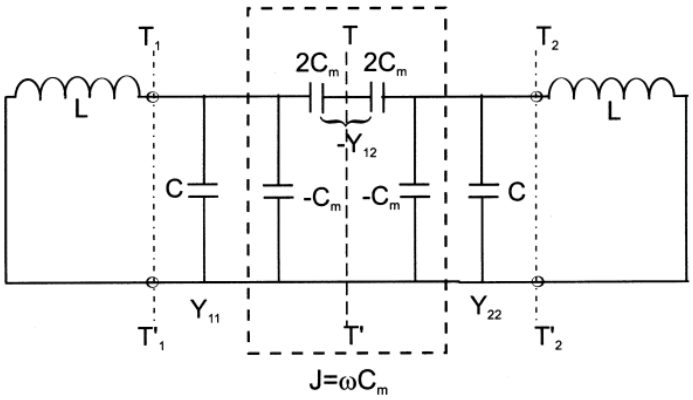


Figure 2.9: Equivalent of Electrical Coupled Circuit [9]

In the odd mode, the electric wall boundary condition is assigned to the symmetry plane in the middle. The normal component of the magnetic field and the tangential component of the electric field are considered to be zero. In this case, the resonant frequency f_E is obtained by considering the short-circuited T-T' as in Equation (2.20).

$$f_E = \frac{1}{2\pi\sqrt{L(C + C_m)}} \tag{2.20}$$

Likewise, when even mode is wanted to be examined, the symmetry plane is considered as a magnetic wall. The normal electric field and tangential magnetic field are both zero in this boundary condition. In this case, the resonant frequency f_M is obtained by considering open-circuited T-T' as in Equation (2.21). As a result, the coupling coefficient is calculated as in Equation (2.22) [9].

$$f_M = \frac{1}{2\pi\sqrt{L(C - C_m)}} \tag{2.21}$$

$$k_E = \frac{f_M^2 - f_E^2}{f_M^2 + f_E^2} = \frac{C_m}{C} \tag{2.22}$$

2.3.2 Magnetic Coupling

There is magnetic coupling if the interaction between two resonators occurs through a magnetic field. This coupling is indicated by L_m in the circuit as in Figure 2.10. In this instance, the circuit is transformed into a symmetrical form, yielding the circuit shown in Figure 2.11.

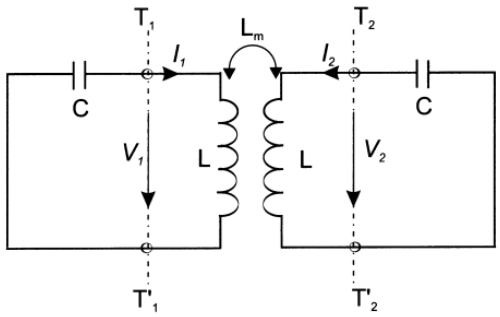


Figure 2.10: Magnetic Coupled Circuit [9]

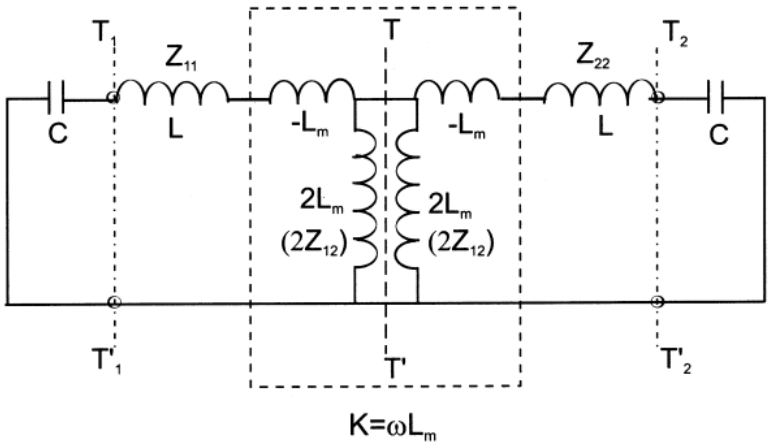


Figure 2.11: Equivalent of Magnetic Coupled Circuit [9]

Even and odd mode analyses provide resonant frequency formulas Equations (2.23) and (2.24), same as in the preceding example. Similarly, the magnetic coupling coefficient k_M is found as in Equation (2.25) [9].

$$f_E = \frac{1}{2\pi\sqrt{(L - L_m)C}} \tag{2.23}$$

$$f_M = \frac{1}{2\pi\sqrt{(L + L_m)C}} \tag{2.24}$$

$$k_M = \frac{f_E^2 - f_M^2}{f_E^2 + f_M^2} = \frac{L_m}{L} \tag{2.25}$$

2.3.3 Mixed Coupling

When electric and magnetic couplings coexist, mixed-coupling happens as in Figure 2.12. In the circuit, self-capacitance, and inductance are represented by the symbols C and L, respectively, whereas mutual capacitance and inductance are represented by the symbols C'_m and L'_m as in Figure 2.13.

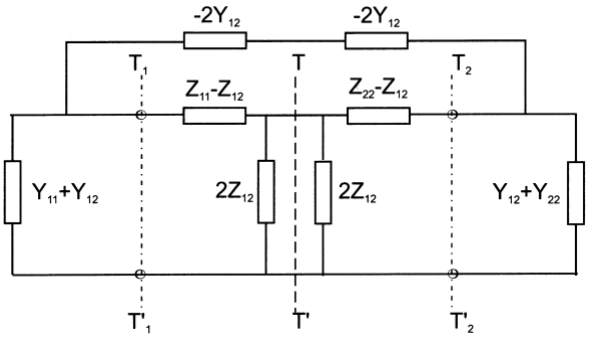


Figure 2.12: Mixed Coupled Circuit [9]

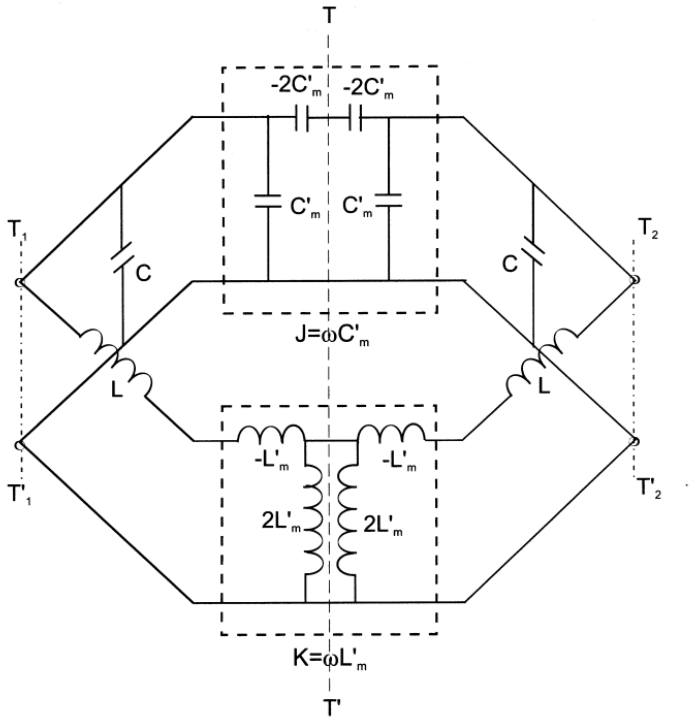


Figure 2.13: Equivalent of Mixed Coupled Circuit [9]

The corresponding formulas for resonant frequencies are found in Equations (2.26) and (2.27). Using the assumption $L'_m C'_m \ll LC$, the mixed coupling coefficient calculation can be approximated as in Equation (2.28) [9].

$$f_E = \frac{1}{2\pi\sqrt{(L - L'_m)(C - C'_m)}} \tag{2.26}$$

$$f_M = \frac{1}{2\pi\sqrt{(L + L'_m)(C + C'_m)}} \tag{2.27}$$

$$k_{MIX} = \frac{f_E^2 - f_M^2}{f_E^2 + f_M^2} = \frac{CL'_m + LC'_m}{LC + L'_m C'_m} \approx \frac{L'_m}{L} + \frac{C'_m}{C} = k'_M + k'_E \tag{2.28}$$

2.4 Filters with Substrate Integrated Waveguide

There are possible construction methods or transmission media types such as waveguides or planar transmission lines for microwave filters. SIW is one of these methods

that is made up of three basic layers which are ground, dielectric, and ground. Then, rows of vias are used for confining the form as can be seen from Figure 2.14.

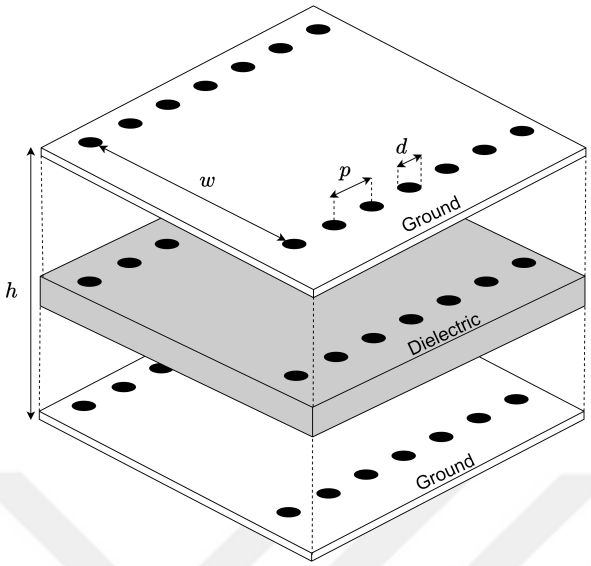


Figure 2.14: SIW Structure

The first parameter to consider during the design is that the distance between the vias that constitute the side wall must be properly calculated by the designer of the SIW structure. In this way, losses because of EM field leakages are prevented. The mentioned situation is achieved by applying the design rules given in [60]. For the SIW structure to be physically designable, the condition in Equation (2.29) specifies that the diameter (d) of the via must be less than the space between the neighboring vias (p). Furthermore, it can be understood from Equation (2.30) that the distance between two consecutive vias should be smaller than a quarter of the cutoff wavelength (λ_c) and bigger than 0.05 λ_c. Additionally, Equation (2.32) shows that there is a limitation for the wave number in a vacuum (k_0) to eliminate leakage loss.

$$p > d \tag{2.29}$$

$$p/\lambda_c < 0.25 \tag{2.30}$$

$$p/\lambda_c > 0.05 \tag{2.31}$$

$$l/k_0 < 1 \times 10^{-4} \tag{2.32}$$

The feasible area of physical dimensions for SIW is presented in Figure 2.15, taking into consideration the previously explained inequalities [60].

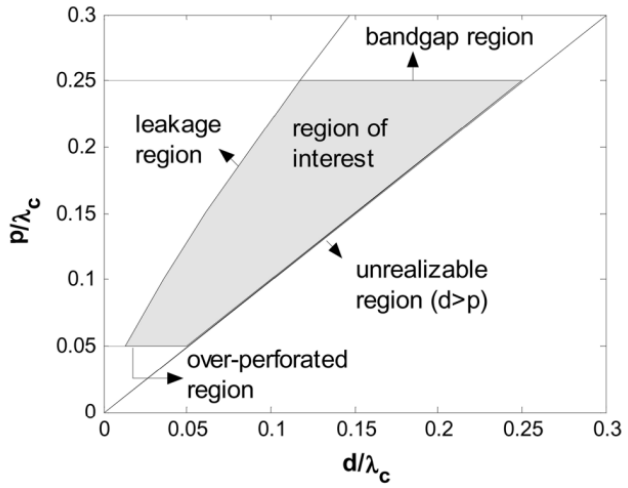


Figure 2.15: Region of Interest for SIW [60]

Another factor to keep in mind during the design process is that the only modes of propagation supported by SIW structures are Transverse-Electric (TE) modes. On the other hand, Transverse-Magnetic (TM) modes are incapable of propagating because of the lack of regular surface current resulting from the discontinuity between the successive vias that constitute the side walls of the SIW. As the height of the structure is typically significantly lower than its width in TE modes, TE_{n0} modes are taken into account with $n = 1, 2, 3, ...$ Thus, of these models, the TE_{10} mode is the fundamental one. The surface current flow for TE_{10} in a SIW structure is depicted in Figure 2.16 [61].

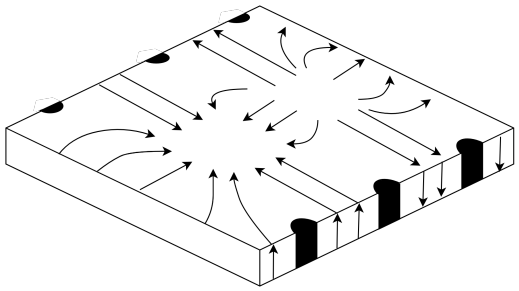


Figure 2.16: Surface Current for TE_{10} of SIW

Conventionally, rectangular waveguides (RWG) and SIW have very much alike characteristics [62]. One example is that the guided wavelength of an EM wave is determined according to physical dimensions in both RWG and SIW structures, and is typically longer than the free space wavelength. Another example is that the cut-off frequency of operation similar to RWG is influenced by dimension selections of the structure. Thus, while establishing the design process, RWG fundamentals can be applied. Additionally, characteristics like the type of dielectric, the diameter of the via, the distance between vias, and manufacturing tolerances influence the structure design.

By using the similarity between RWG and SIW, resonant frequency calculation can be made for TE modes for the designed structure. The correlation between the dimensions of SIW structures and RWG effective width has been experimentally deduced considering similar propagation characteristics. Equations (2.33), (2.34), and (2.35) are some of these proposed equations [63]. Basic waveguide effective width (w_{eff}) computation is included in Equation (2.33). However, as the d value increases, this formula becomes inapplicable. Equation (2.34) should be applied when $p/d < 3$ and $d/w < 0.5$. Equation (2.35) is another w_{eff} calculation that can be worked with.

$$w_{eff} = w - \frac{d^2}{0.95p} \tag{2.33}$$

$$w_{eff} = w - 1.08\frac{d^2}{p} + 0.1\frac{d^2}{w} \tag{2.34}$$

$$w = \frac{2w_{eff}}{\pi} cot^{-1}(\frac{\pi p}{4w_{eff}} ln\frac{p}{2d}) \tag{2.35}$$

SIW can be used to generate a cavity form. The fundamental mode of this cavity is TE_{101} if its length (u) is greater than its width, which is greater than its height. The calculation of u_{eff} is the same as that of w_{eff}, according to Equations (2.36) and (2.37). Equation (2.38) expresses how to determine the resonant frequency of the SIW cavity using these data [64].

$$u_{eff} = u - \frac{d^2}{0.95p} \tag{2.36}$$

$$u_{eff} = u - 1.08\frac{d^2}{p} + 0.1\frac{d^2}{u} \tag{2.37}$$

$$f_{101} = \frac{c_0}{2\pi\sqrt{\mu_r\epsilon_r}}\sqrt{\left(\frac{\pi}{w_{eff}}\right)^2 + \left(\frac{\pi}{u_{eff}}\right)^2} \tag{2.38}$$

The third aspect that should be taken into consideration during the design is the elements that may cause potential losses. SIW exhibits conductor losses (α_c) and dielectric losses (α_d) in the same way as RWG. Consequently, decisions that would increase losses should be avoided wherever possible for an efficient design. Relevant loss equations for RWG can be found in Equations (2.39), and (2.40) by implementing Equations (2.41), (2.42) as explained in [65]. The phase constant β, the dielectric loss tangent $tan\delta$, the intrinsic impedance η, the metal conductivity σ, and the free space wave number k are all represented in the equations.

$$\alpha_{d,RWG} = \frac{k^2 tan\delta}{2\beta} \tag{2.39}$$

$$\alpha_{c,RWG} = R_s\frac{2h\pi^2 + w^3k^2}{w^3h\beta k\eta} \tag{2.40}$$

$$\eta = \sqrt{\frac{\mu_0}{\epsilon_0\epsilon_r}} \tag{2.41}$$

$$R_s = \sqrt{\frac{2\pi f\mu_0}{2\sigma}} \tag{2.42}$$

Loss equations for SIW at a frequency f are examined in Equations (2.43) and (2.44) as suggested in [66].

$$\alpha_{c,SIW}(f) = \frac{\sqrt{\pi f\epsilon_0\epsilon_r}}{h\sqrt{\sigma}} \times \frac{1 + 2(f_0/f)^2(h/w_{eff})}{\sqrt{1-(f_0/f)^2}} \tag{2.43}$$

$$\alpha_{d,SIW}(f) = \frac{\pi f\sqrt{\epsilon_r}}{c_0\sqrt{1-(f_0/f)^2}}tan\delta \tag{2.44}$$

CHAPTER 3

SIW BANDPASS FILTER DESIGN

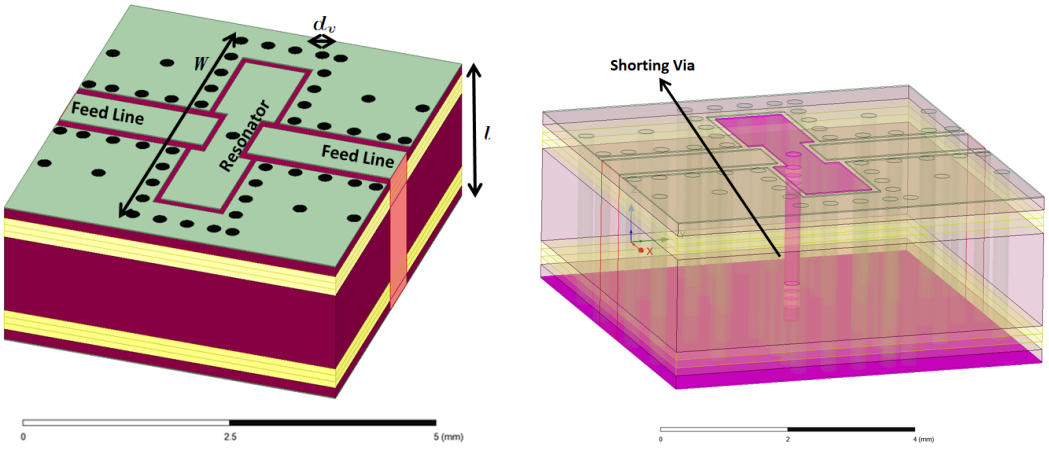
The quasi-lumped SIW filter design technique is chosen as an optimum solution because it offers the required wide BW and high out-of-band suppression with significantly smaller dimensions than a filter typically manufactured with lumped elements or distributed elements solely [67, 68].

First of all, the resonator form is studied from different perspectives. Afterward, utilizing Section 2.2 filter basics and Section 2.4 SIW basics, a fourth-order bandpass filter is developed in accordance with the intended specifications. EM simulations of the designed filter are done with HFSS [54]. A layout drawing program called Mentor PADS is used to draw the designed filter, and the relevant files (Gerber, drill, and board outline) with the planned stack up are used to manufacture it. The generated design is then measured using a vector network analyzer (VNA). Results from measurements and simulations are compared.

3.1 Resonator Design

The resonator structure, which serves as the foundation for the bandpass filter, is examined at the beginning. The resonant frequency (ω_r) is the first crucial parameter for this structure that has to be investigated. The frequency at which the stored magnetic energy (W_m) and electric energy (W_e) of the resonator equal each other, i.e. $W_m = W_e$, is known as the ω_r. Due to this equality between the stored energies, the imaginary elements in the impedance cancel each other. Thus, a highly efficient energy transfer occurs between the input and output ports. This corresponds to the peak point in the S_{21} response of the structure in most cases. Considering parallel resonant

circuits are employed in this investigation, the inductance (L) and capacitance (C) values of the resonator connected in shunt are the two main parameters to establish the ω_r. It can be calculated as $\omega_r^2 = 1/(L \times C)$. Figure 3.1 illustrates the resonator structure that is studied.



(a) Resonator (b) Shorting Via

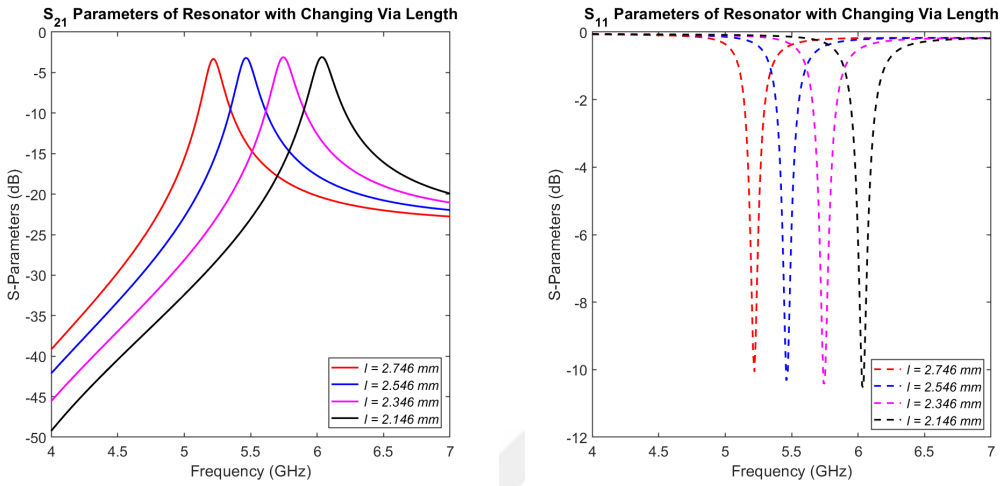
Figure 3.1: Resonator Structure

While the capacitance of the resonator structure is because of the gap between parallel conductors which are the resonator plane and the ground, the inductance value of it is formed by the via connecting the parallel conductor plane to the ground plane in the designed resonator. The calculation of the inductance value can be seen in Equation (3.1) where η_0 is the wave impedance and c_0 is the speed of light in a vacuum. In order to apply this inductance formula, the stack-up thickness (l) must be much less than a quarter of the guided wavelength value i.e. $l << \lambda/4$. If this requirement is satisfied, the plated via can be conceptualized as a short stripline positioned perpendicular to the ground.

$$L = \frac{\eta_0 l}{2\pi c_0} ln\left(\frac{4W}{\pi d_v}\right) \tag{3.1}$$

The formula in Equation (3.1) makes clear that the change in inductance value is caused by a number of distinct factors [68]. Parametric sweep simulations are performed separately for each factor and the results are examined. The first of these is

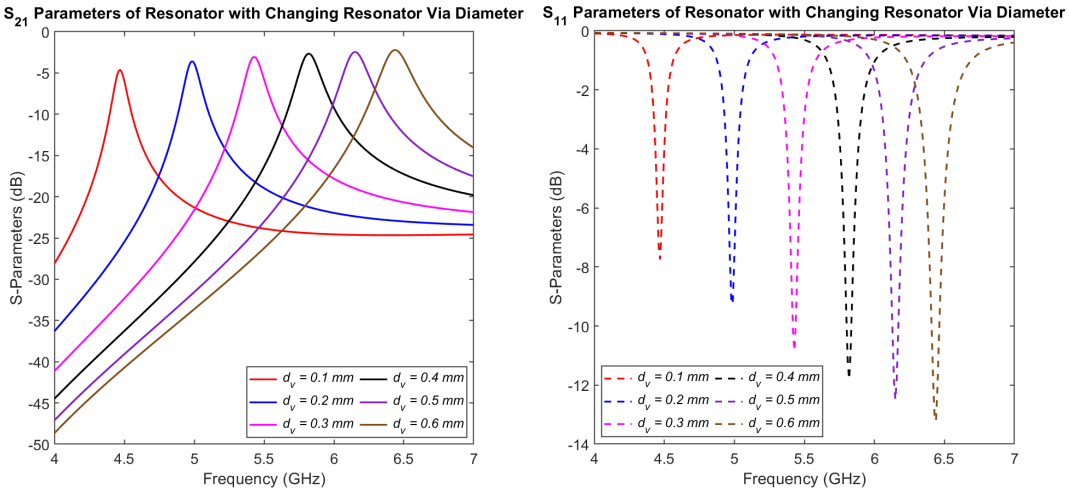
the length of the via, or in other words, the thickness of the stack up. The resonant frequency drops as the inductance value increases with this thickness (l) which is shown in Figure 3.2.



(a) S_{21} Parameters (b) S_{11} Parameters

Figure 3.2: S-Parameters of Resonator with Changing Via Length

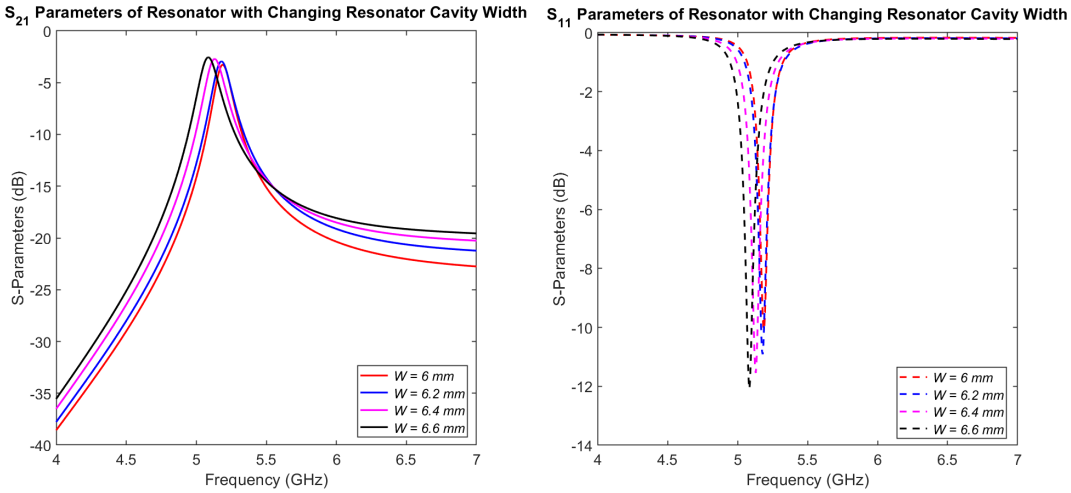
The diameter of the via (d_v) is another factor. The resonant frequency increases as the via diameter widens and the inductance value falls as shown in Figure 3.3.



(a) S_{21} Parameters (b) S_{11} Parameters

Figure 3.3: S-Parameters of Resonator with Changing Via Diameter

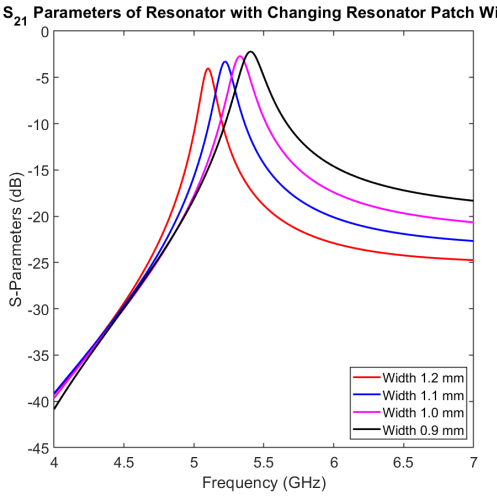
Lastly, the size of the cavity (W) is directly proportional to its inductance value. For this reason, as the cavity grows, the resonant frequency decreases. The simulation results in Figure 3.4 also confirm this statement.



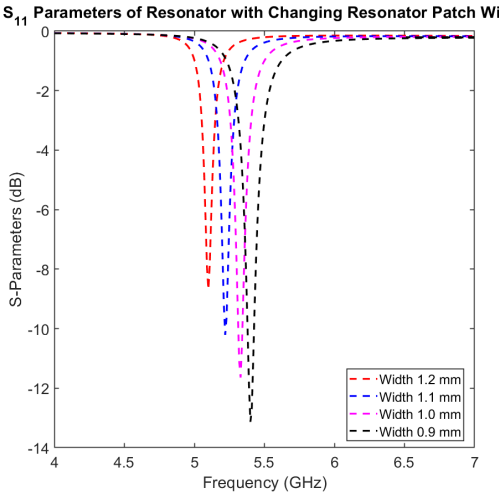
(a) S_{21} Parameters (b) S_{11} Parameters

Figure 3.4: S-Parameters of Resonator with Changing Cavity Width

The capacitance value between the resonator and the ground at the bottom layer increases as the patch dimensions of the resonator increase. Likewise, as the gap between the resonator and the surrounding ground decreases, the capacitance value increases. The increase in capacitance leads to a decrease in the resonant frequency. All of these changes have been verified by simulation with the help of parametric analyses. The plots in Figures 3.5, 3.6, and 3.7 verify the change of resonant frequency according to the three critical parameters explained.

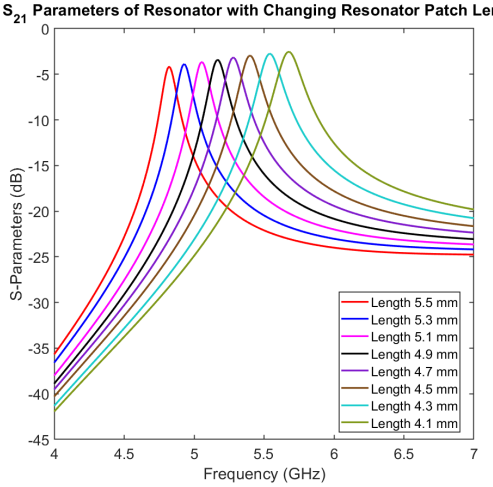


(a) S_{21} Parameters

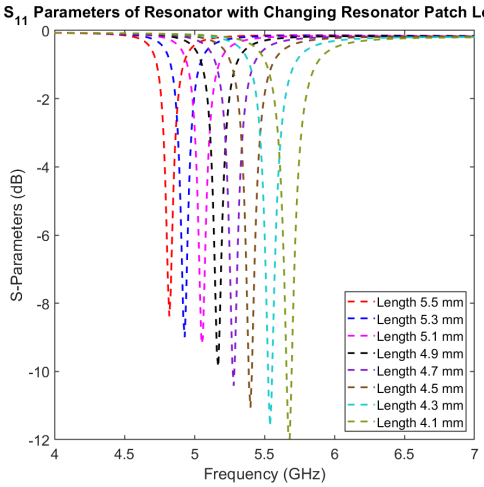


(b) S_{11} Parameters

Figure 3.5: S-Parameters of Resonator with Changing Patch Width

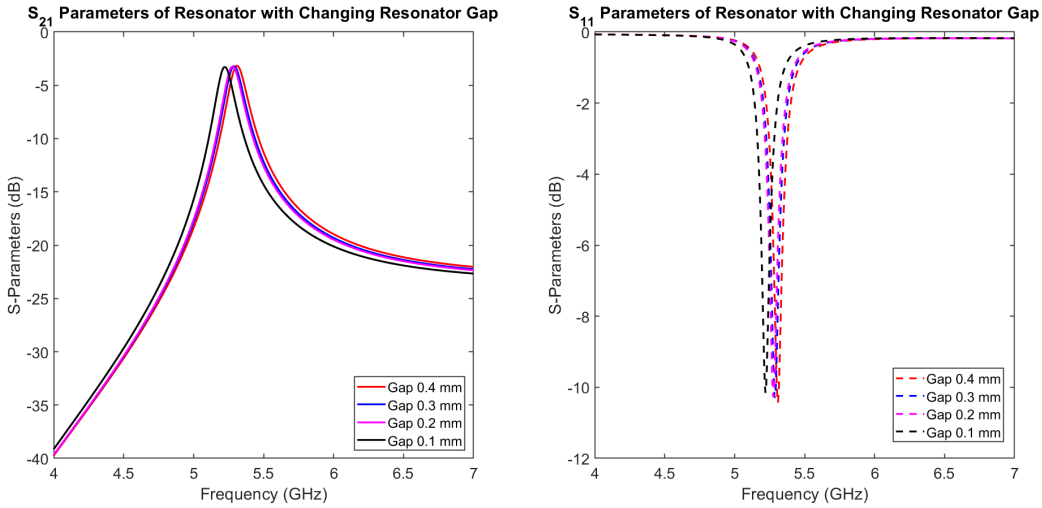


(a) S_{21} Parameters



(b) S_{11} Parameters

Figure 3.6: S-Parameters of Resonator with Changing Patch Length



(a) S_{21} Parameters

(b) S_{11} Parameters

Figure 3.7: S-Parameters of Resonator with Changing Gap

The second parameter that forms the characteristic of a resonator is the quality factor (Q). It shows the ratio of the average EM energy the resonators can store to energy loss per second. Equation (3.2) shows the Q factor definition in a formalized form. The loss may be because of numerous reasons such as dielectric loss, radiation loss, and conductor loss. It can be said that the Q factor of a low-loss resonator is higher [58].

$$Q = \omega \frac{W_m + W_e}{P_{loss}} \tag{3.2}$$

For parallel resonant circuits Equations (3.3), (3.4), and (3.7) can be utilized for energy calculation. R is the resistance of the resonator. I_L denotes the current passing through the inductor [58].

$$P_{loss} = \frac{1}{2}\frac{|V|^2}{R} \tag{3.3}$$

$$W_e = \frac{1}{4}|V|^2 C \tag{3.4}$$

$$W_m = \frac{1}{4}|I_L|^2 L \tag{3.5}$$

$$= \frac{1}{4}|\frac{V}{Lj\omega}|^2 L \quad \text{(apply } V = Lj\omega I_L \text{)} \tag{3.6}$$

$$= \frac{1}{4}|V|^2 \frac{1}{\omega^2 L} \tag{3.7}$$

At the resonant frequency, one can rewrite the Equation (3.2).

$$Q_0 = \omega_r \frac{2W_m}{P_{loss}} \quad \text{(apply } W_m = W_e\text{)} \tag{3.8}$$

$$= \omega_r \frac{2\frac{1}{4}|V|^2 \frac{1}{\omega_r^2 L}}{\frac{1}{2}\frac{|V|^2}{R}} \tag{3.9}$$

$$= \frac{R}{\omega_r L} \tag{3.10}$$

It turns out that the Q factor in Equation (3.10) can also be computed as the ratio of the resonant frequency to half-power BW when certain approximations are made in the input impedance calculation for frequencies near the resonant frequency [69]. In the dB scale S parameter graph, half power occurs at frequencies 3 dB below the resonant frequency. This approach is used to find the Q value of the designed resonator structure whose characteristic is simulated during the design. As the cavity size, capacitive gap, and via diameter increase the Q factor increases. On the other hand, the dielectric thickness and resonator length are inversely proportional to the Q factor value.

The value of the Q parameter varies depending on the structure to which the resonator is connected. The Q factor in Equation (3.10), which is calculated by considering a simple resonator that is not connected to any external circuit, is called the unloaded quality factor (Q_U). In case it is combined with another circuit with load resistance R_L, it is necessary to mention the loaded Q factor (Q_L). The loaded Q factor is calculated as expressed in Equation (3.11). The Q factor of the other circuit to which the resonator is combined has an external quality factor (Q_e). When the load is connected to the parallel resonator, Q_e is obtained as in Equation (3.12).

$$\frac{1}{Q_L} = \frac{1}{Q_e} + \frac{1}{Q_0} \tag{3.11}$$

$$Q_e = \frac{R_L}{\omega_r L} \tag{3.12}$$

While selecting the dimensions of the parameters in the resonator during the BPF design, an attempt is made to ensure that the appropriate resonant frequency and the appropriate Q_U. As previously mentioned, a trade-off between several parameters affecting filter performance must be made. If this study examined specifically, increasing the resonator size increases the Q_U value and causes a decrease in the resonant frequency. It also causes growth in size which is not desired. Because of this, an improvement in the Q can be obtained without significantly increasing the resonator size by modifying other factors, such as the length of the patch.

There are many factors that are taken into consideration when designing a filter in the thesis. First, the fundamental SIW equations are used to minimize the radiation loss. As can be seen from the Region of Interest graph in Figure 2.15 and related equations, reducing the via radius increases the bandgap. For this reason, the via diameter of the SIW structure is selected as 0.25 mm, taking into account the manufacturing limits. The vias that make up the SIW walls are positioned at intervals of 0.25 mm. The two walls are spaced 5.75 mm apart. One of the reasons SIW is recommended in filter design is that it does not permit TM mode propagation, as discussed in Section 2.4. This prevents some mode-related issues, like out-of-band parasitic effects. Another purpose of the SIW structure in the design is to ensure that the quasi-lumped filter structure is shielded from the outside world.

The dielectric thickness is determined as thick as possible because of its couple of benefits. The first one is to increase the inductance value of the resonator so that the required capacitance value for ω_r becomes low. This enables smaller patch sizes and compact design. Meanwhile, it is considered not to exceed the manufacturing limitations. The smallest feasible via diameter which is 0.25 mm for the resonator is used because of the same reasons with dielectric thickness. manufacturing ease is ensured throughout the design by utilizing this diameter value in all existing vias. The size of

the patch is chosen once the inductance value of the resonator has been established, as this information provides the necessary capacitance value. The width and length of the resonator patch are determined to be 1.1 mm and 4.8 mm, respectively.

Another element to consider in the design is the characteristic impedance value of the grounded coplanar waveguide located at the beginning and end of the filter. After the stack-up thickness and the dielectric materials to be used are determined, studies are carried out to ensure the matched condition at both ports of the filter so that power transfer before and after the filter can be provided most efficiently. In other words, there are fewer signal reflections between two distinct components. Furthermore, by constructing the filter with 50 ohms, it has become generally usable and compatible with the majority of RF systems, as most of them utilize 50 ohms. The standard impedance in the RF field is determined as 50 ohms since studies have shown that this value offers adequate power management and signal integrity performance in a conveniently producible manner. Since having two types of materials in the stack increases the complexity, a parametric sweep is made for various width values by utilizing the Ansys Q2D tool [70]. The optimum result is achieved with 0.9 mm coplanar width and 0.2 mm gap to the ground. Figure 3.8 displays the results of the performed parametric analysis.

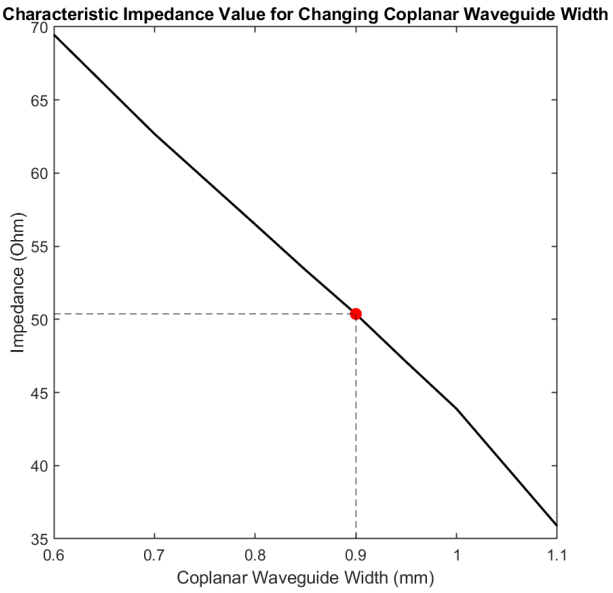


Figure 3.8: Characteristic Impedance Value for Changing Coplanar Waveguide Width

3.2 BPF Design Specifications

The design criteria of the targeted filter can be found in Table 3.1. The BW and cut-off frequencies of the intended filter are decided by the frequency planning of the channelized receiver. The second and third harmonics of the frequencies inside the passband are suppressed as much as possible during frequency planning to prevent them from passing through the filter. To illustrate, consider that the frequency at 7GHz, which is twice the lower cutoff frequency, is effectively suppressed by more than 20 dB. This keeps strong power level signals from emerging on the receiver line at the start of the strip.

Table 3.1: Design Specifications of BPF

	Frequency Range	Specification
Insertion Loss	3.5 - 6 GHz	< 2 dB
Return Loss	3.5 - 6 GHz	> 10 dB
Lower Side Rejection	DC - 3 GHz	> 20 dB
High Side Rejection	7 - 13 GHz	> 20 dB

3.3 BPF Design

The center frequency and FBW values required for filter design are obtained using Equations (2.9) and (2.10) according to the given frequency specifications. Considering ω_1 is 3.5 GHz and ω_2 is 6 GHz, ω_0 is calculated as 4.58 GHz. The obtained ω_0 is used to find Δ which is 0.5458. Since the value calculated is greater than 25%, it can be concluded that the filter that needs to be designed is a wideband filter.

As mentioned in Chapter 2, it is decided to use the Chebyshev filter design because of its effective out-of-band suppression, straightforward design, and other features in order to meet the necessary requirements. Moreover, the filter specifications make clear how important it is to have at least a 20 dB suppression at 7 GHz. To achieve this, the order of the filter should be determined appropriately. First, the specified 7 GHz frequency must be converted to normalized low pass format with frequency conversion using the Δ and ω_0 values found. Equation (3.13) expresses this computa-

tion and 1.601 is found as the resulting value. Then, $\left|\frac{\omega}{\omega_c}\right| - 1$ expression is calculated where ω_c is 1 rad/sec. The result is obtained as 0.601. Afterward, it is necessary to determine the corresponding order value from the 0.5 dB ripple plots. The necessary 20 dB suppression amount can be obtained using at least a 4th-order filter, as indicated in Figure 2.2. Following that, the element values required for the 4th-order filter are identified with the help of Table 2.1.

$$\omega \leftarrow \frac{1}{\Delta}\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right) \tag{3.13}$$

The J values that are needed to convert the filter into an admittance inverter BPF configuration are computed using the obtained element values. Table 3.2 shows these characteristic admittance values.

Table 3.2: Calculated Characteristic Admittance Values

$J_{0,1}$	$J_{1,2}$	$J_{2,3}$	$J_{3,4}$	$J_{4,5}$
0.01059	0.00663	0.00557	0.00663	0.01059

Following that, in order to apply the obtained J values in the real design, the necessary coupling coefficient values are reached by using Equation (3.14) [9]. Equation 3.15 shows the resultant values.

$$k_{ij} = \frac{J_{i,j}}{\omega_0 C} = \frac{\Delta}{\sqrt{g_i g_j}} \tag{3.14}$$

$$|k_{ij}| = \begin{bmatrix} 0 & 0.387 & 0 & 0 \\ 0.387 & 0 & 0.325 & 0 \\ 0 & 0.325 & 0 & 0.387 \\ 0 & 0 & 0.387 & 0 \end{bmatrix} \tag{3.15}$$

Additionally, the Q_e value of the designed filter can be obtained using J values as in Equation (3.16). The Q_e value for the designed filter is found to be 3.0603.

$$Q_e = \frac{Y_0 C_r \omega_0}{J_{i,j}^2} = \frac{g_i g_j}{\Delta} \tag{3.16}$$

Consequently, in order to achieve the intended k and Q_e values in the filter design, the impact of every parameter is investigated in Sections 3.4 and 3.5. The intended k value is taken into consideration when choosing appropriate physical values and lumped elements, and the final version of the filter is created as in Figure 3.9. The series lumped capacitances are 0.9 pF for the first and fifth capacitances, 0.3 pF for the second and fourth capacitances, and 0.5 pF for the third capacitance. Two 0.1 pF ground capacitors are also positioned symmetrically for each of the four resonators.

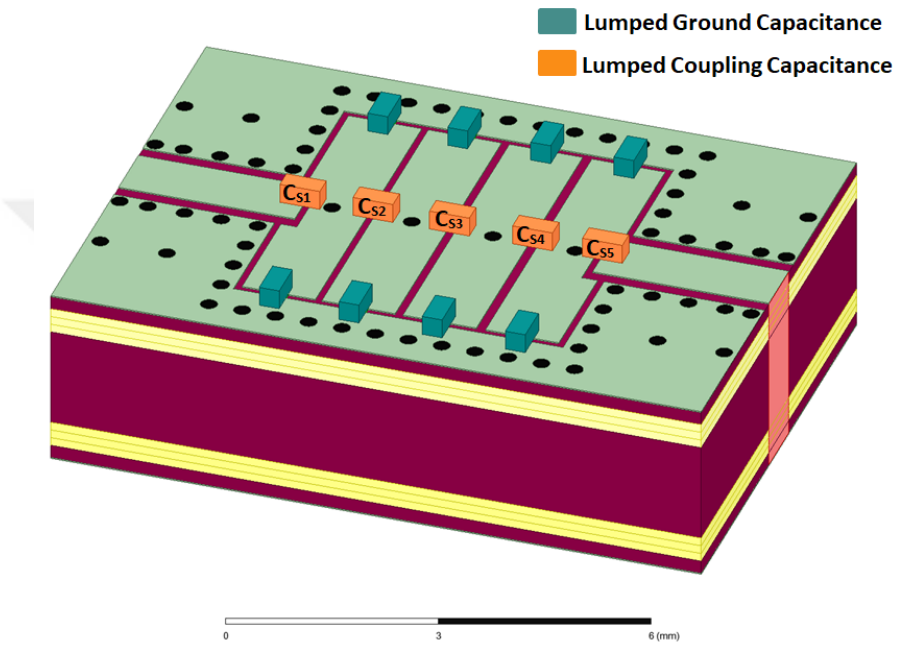
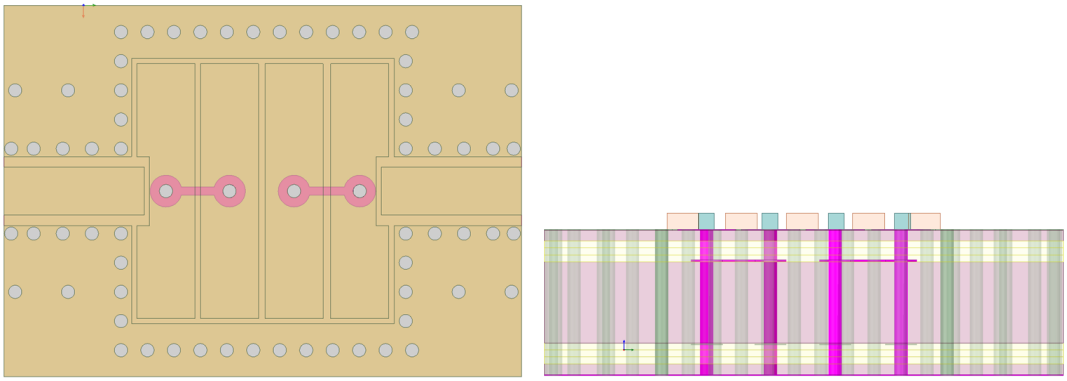


Figure 3.9: Designed BPF

The intermediate layer of the filter is displayed in Figure 3.10 from both the top and front view along with the locations of the highlighted short circuit lines. Short circuit lines are positioned to the intermediate layer to introduce magnetic coupling between resonators, while capacitances between resonators provide electrical coupling. Section 3.4 provides a more comprehensive investigation of the coupling mechanisms of the design. There is 1.22 mm between the centers of the rings at either end of the lines in the intermediate layer. Moreover, the line has a width of 0.15 mm. The rings have a radius of 0.3 mm. Resonators are spaced 0.1 mm apart from one another and from the ground.



(a) Top View (b) Front View

Figure 3.10: Short Circuit Line Forms in Designed BPF

The filter design has a multilayer structure in its layout stackup. The top and bottom layers have 34 um thick plating and 18 um thick copper, as can be seen in Figure 3.11. The dielectric materials for the first, third, and fifth cores are chosen as RO4003, whereas the second and fourth cores are utilized as FR4. The main reason for employing RO4003 rather than FR4 under conductor planes is that the former has a lower loss tangent (about 0.0027 at 10 GHz) and dielectric constant (roughly 3.38 at 10 GHz) than the latter (approximately 0.02 and 4.5 at 10 GHz, respectively). As a result, transmission can be accomplished more efficiently and with less RF signal attenuation. Furthermore, prepreg layers are utilized as an adhesive layer to hold cores together during lamination and facilitate PCB manufacturing. Prepreg layers also aid in customizing the overall thickness of the board. To improve the thickness of the PCB, a thicker third core is selected. Segments of short circuit lines are positioned in the second copper layer.

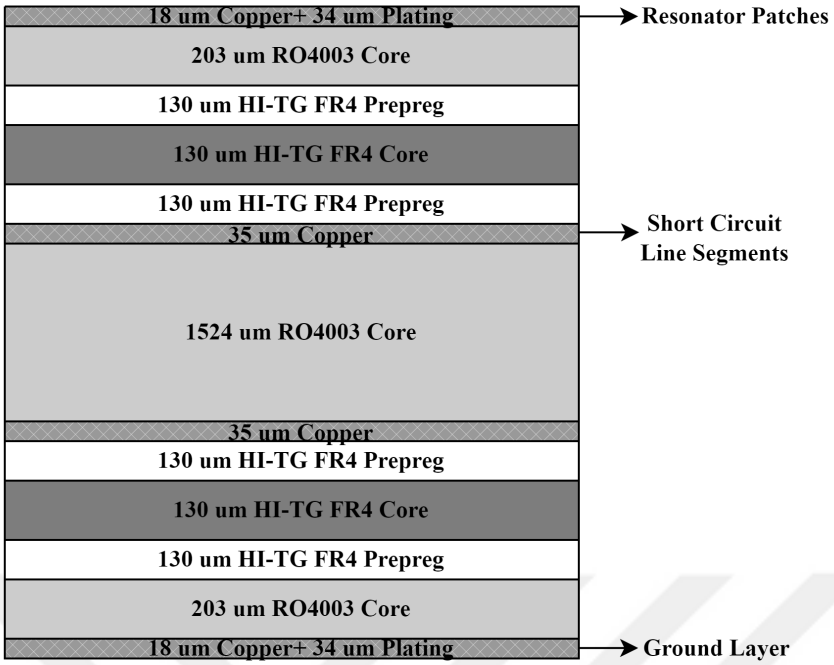


Figure 3.11: Stackup of Designed BPF

3.4 Coupling Analysis of Designed Filter

Considering each of the 4 stages that make up the filter as a resonator, it is planned to create the admittance inverters and hence the filter characteristic by taking advantage of the coupling mechanisms between these resonators, and also between feed lines and resonators. For this reason, after the resonator structure and design parameters such as J values, order of the filter, stack up, etc. are established, coupling coefficient determination studies are carried out to create the desired BPF design. Given the large BW of the desired filter, the mixed coupling is intended to introduce additional transmission zeros (TZs). These additional TZs allow for the necessary level of out-of-band suppression to be guaranteed in a smaller area. Additionally, TZ locations can be adjusted at a higher resolution, including the two stopband sides of the band: upper and lower.

A dual resonator design, as shown in Figure 3.12, is utilized to examine the coupling strength between resonators, and an investigation is carried out to extract the physical counterparts of the coupling coefficient values.

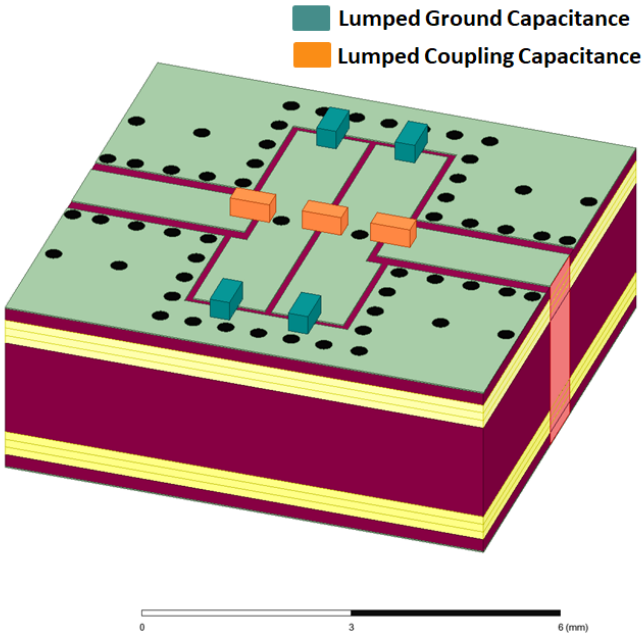


Figure 3.12: Dual Resonator Design

To derive coupling information from physical attributes, the capacitances that allow external coupling are set to 0 pF. This makes it possible to identify frequency peak (f_p) values in the frequency response of the weakly coupled filter instance. These frequency peaks can be represented by f_e or f_m, depending on whether they are caused by electrical or magnetic coupling. Then, as the derivations in Section 2.3 demonstrate, the coupling coefficient value for synchronously tuned resonators can be calculated as in Equation (3.17), where f_{p1} and f_{p2} are equivalent to either f_e or f_m based on the design [9].

$$k = \pm \frac{f_{p2}^2 - f_{p1}^2}{f_{p2}^2 + f_{p1}^2} \tag{3.17}$$

Electrical coupling (k_E) results from the capacitive gap between the resonators. In order to generate the necessary capacitive gap in less area, lumped capacitors are also utilized. An additional benefit of this application is that when the filter needs to be tuned later, the capacitance value can be easily changed by replacing it with a component of the same package size. Short circuit lines between the first and second resonators and the third and fourth resonators are created through the intermediate layer to create magnetic coupling (k_M). In this case, the sum of the electric and

magnetic couplings almost equals the total amount of coupling as it is explained in Equation (3.18).

$$k_{total} \approx k_E + k_M \tag{3.18}$$

The coupling mechanisms whose effects on the design are examined are shown in Figure 3.13. The dielectric layers are hidden for demonstration purposes. The impact of all kinds of physical design parameters on the k value is assessed. The optimal physical dimensions are then ascertained for the intended k_{total} value.

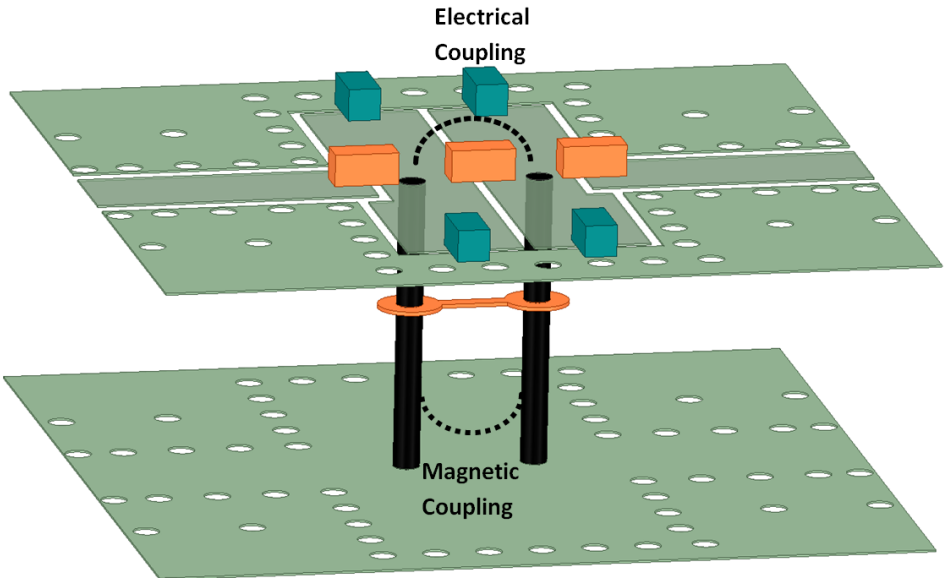


Figure 3.13: Coupling Structures of Dual Resonator Design

The first factor which has an impact on the k_M value is the width of the short circuit line. The cross-sectional area through which current flows expands with width. As a result, magnetic coupling strengthens and magnetic fields can interact more. Figure 3.14 illustrates how k_{total} increases with increasing width as the distance between the frequency peak values grows.

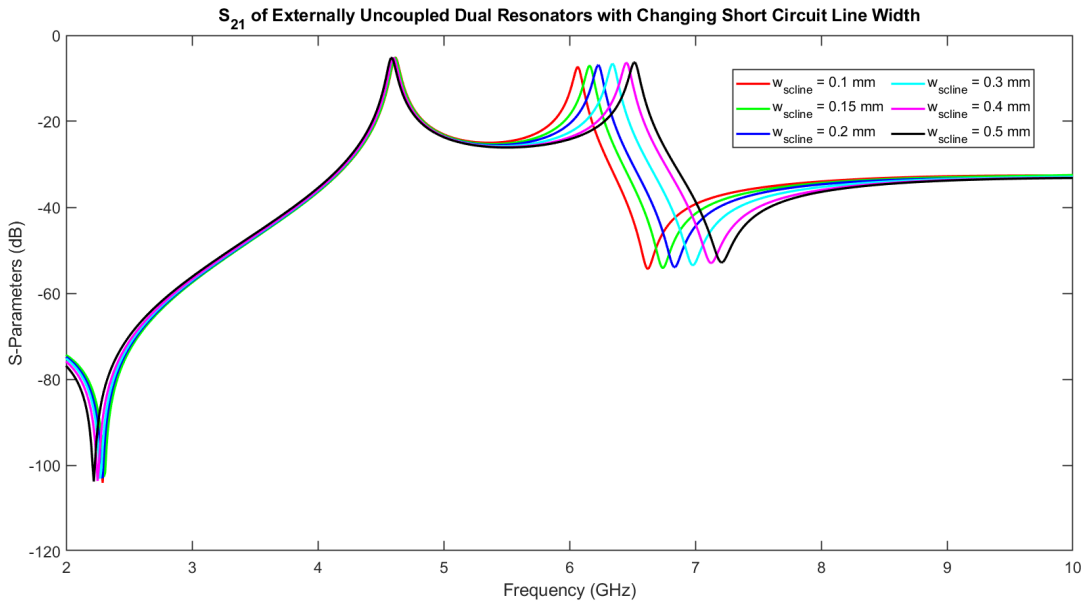


Figure 3.14: S-Parameters of Externally Uncoupled Resonators with Changing Short Circuit Line Width

The separation of the resonator vias is the second parameter whose impact is investigated. The simulation results show that the magnetic coupling increases with decreasing distance when the distance is varied in 0.05mm steps as in Figure 3.15. The reason behind this is that the large distance between two shorting vias reduces the interaction of the magnetic fields around them. At the same time, it causes a slight increase in the resistance of the short circuit line, which lowers the current flowing through it. This again results in a decrease in the magnetic coupling.

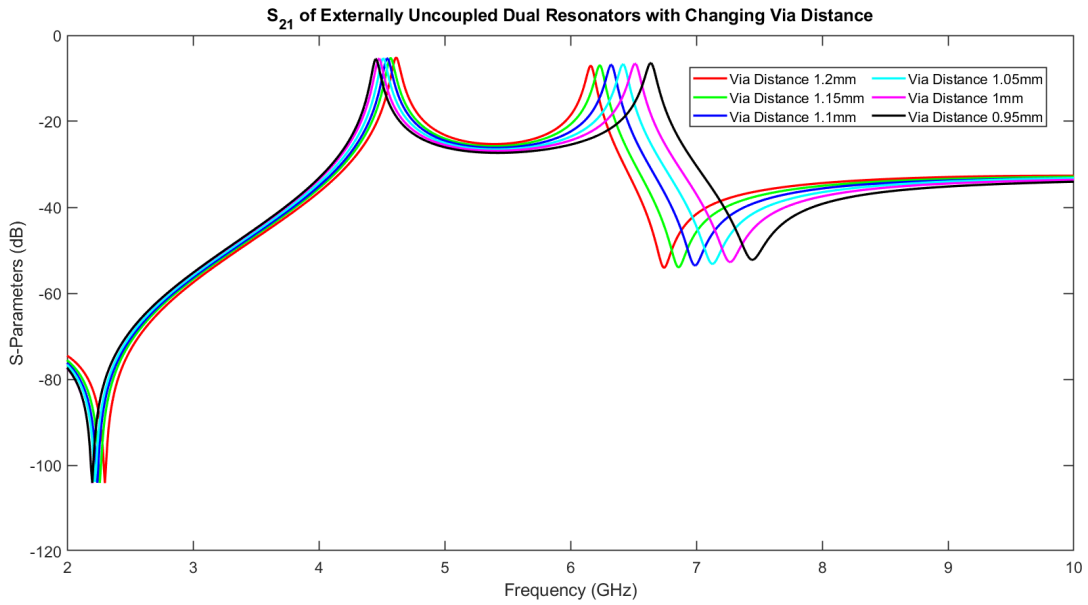


Figure 3.15: S-Parameters of Externally Uncoupled Resonators with Changing Via Distance

The layer at which the short circuit line is positioned is the third component that affects the k_M value. In order to observe this effect, the short circuit line is positioned in two different layers with a distance of 130 µm between them, and its effect on the uncoupled dual resonators is observed. As interpreted from Figure 3.16, the distance between f_p values and, consequently, k_M increases for the short circuit line response in the upper layer. This is because the short circuit line on the upper layer creates a shorter path through which the current can flow. This causes the magnetic fields to become more concentrated, and the magnetic coupling is strengthened.

Another parameter whose effect is examined is the capacitance value that provides electrical coupling. The electrical coupling level between two resonators increases as the capacitance increases. Even though it is not as effective as the lumped capacitor, k_E can also be increased by reducing the interresonator spacing. Moreover, as the electrical coupling increases, the distance between the resonant peak frequencies decreases which can be seen from Figure 3.16. However, Equation (3.17) makes it clear that when coupling increases, two peak values should be farther apart and have a deeper section between them. This relation is always valid when only one of the electrical or magnetic couplings exists in the design. In the case of mixed-coupling, it

may not be valid. One coupling type often has a greater value and is dominant than the other in mixed-coupling cases. If non-dominant coupling increases, k_{total} decreases and f_p values approach each other. In this design, which also uses mixed-coupling, the magnetic coupling is stronger than the electrical coupling. For this reason, k_{total} drops as k_E increases because the couplings cancel each other because of the greater dominance of k_M.

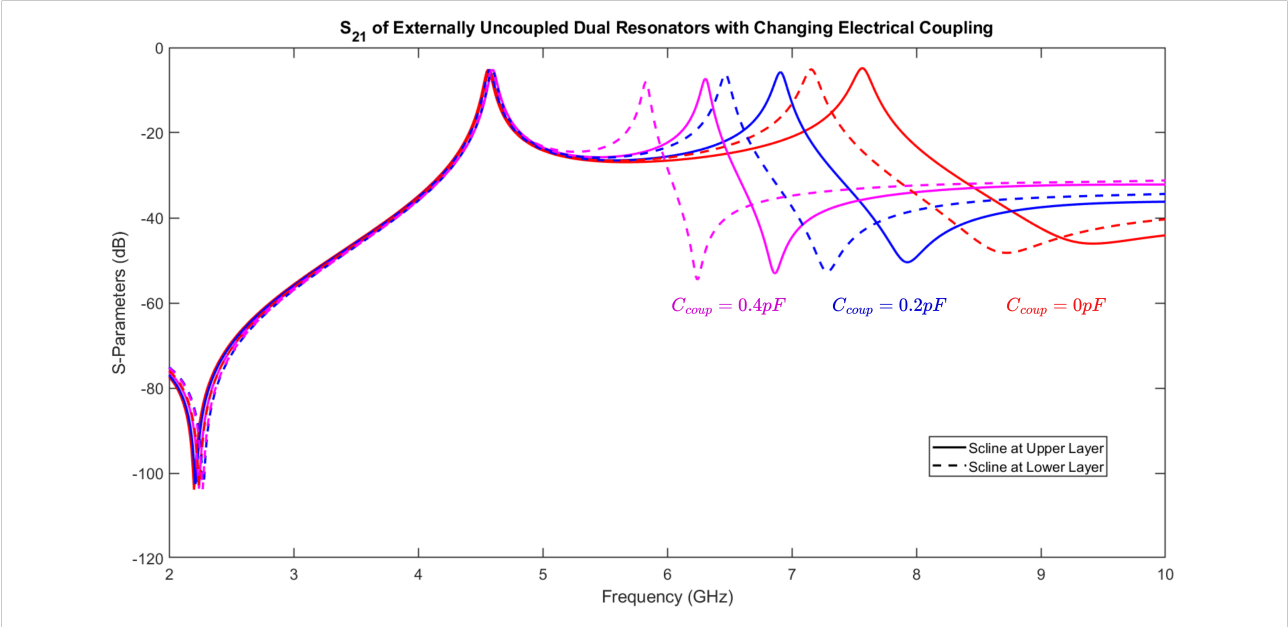


Figure 3.16: S-Parameters of Externally Uncoupled Resonators with Changing Electrical Capacitance and Short Circuit Line Layer

Numerous conclusions are retrieved from the conducted simulations. The first of these states that if the magnetic coupling is greater than electrical coupling (i.e. $k_{total} > 0$), TZ is located at the higher stopband and shifts to higher frequencies as magnetic coupling increases. As a result, both the BW of the filter and absolute value of k_{total} increase. Conversely, in cases where the electrical coupling surpasses the magnetic coupling (i.e., k < 0), TZ appears at the lower stopband. Then, the shift of TZ to lower frequencies and expansion of BW occur with increasing electrical coupling. It is noteworthy that the k_{total} drops as the other coupling value increases and the dominant coupling stays constant. This is because the signs of the k values are opposite for each coupling type and cancel each other out. As a consequence, TZ shifts towards frequencies in the opposite direction and BW decreases.

3.5 Group Delay Analysis of Designed Filter

The output signal experiences a delay in comparison to the input signal whenever a signal passes through a frequency-selective network, like a filter. There are two different delay definitions that could potentially be used to assess this case. The first one is known as phase delay and, refers to the signal delay that a steady sinusoidal signal experiences while being transmitted from the input port to the output port. The phase delay is calculated as given in Equation (3.19), where ϕ is in radians and ω is in radians per second. The second definition is group delay, or the envelope delay, as in Equation (3.20) [9].

$$\tau_p = -\frac{\phi_{21}}{\omega} \tag{3.19}$$

$$\tau_d = -\frac{d\phi_{21}}{d\omega} \tag{3.20}$$

A wideband signal that exhibits a flat group delay response preserves the features of the signal by introducing an equal amount of phase delay into each of its frequency elements. Because of this, it is another parameter that needs to be taken into account while designing filters. Figure 3.17 demonstrates how the group delay varies with the external coupling capacitance. Delay changes in the pass band, cut-off frequencies, and transition band are of special interest. The response flattens and the group delay decreases as the external coupling capacitance increases, as Figure 3.17 indicates. However, the growth in capacitance begins to have less impact after a certain point.

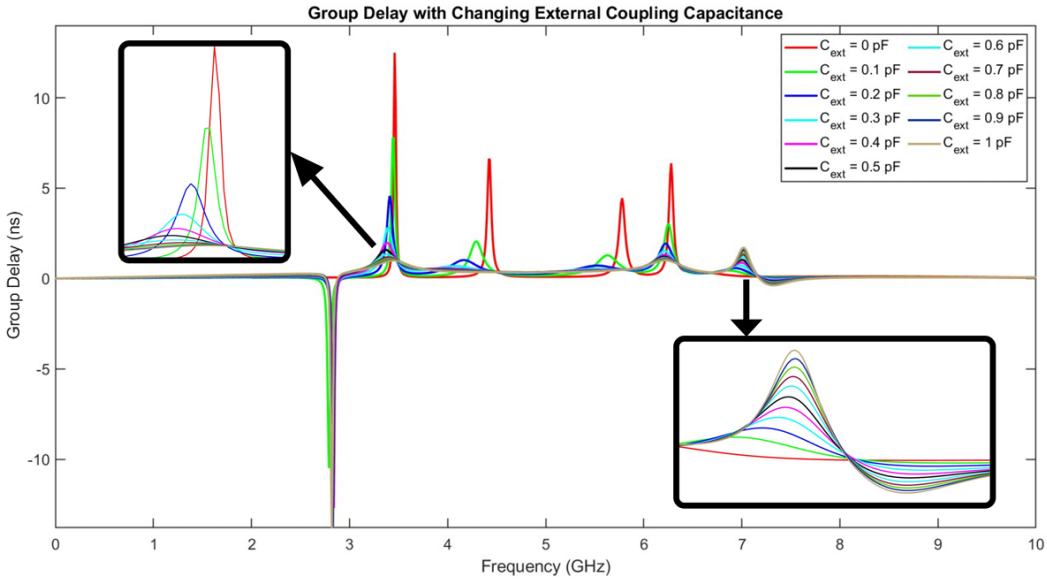


Figure 3.17: Group delays with Changing External Coupling Capacitance

3.6 Simulation Results

Figure 3.18 shows the simulation result of the filter designed in line with the specified parameter dimensions and optimized with the help of simulations. As a result of the study, a filter complying with the design goals is obtained successfully. As can be seen from the marked data points, the filter has a maximum IL of 0.71 dB in the band between 3.5 GHz - 6 GHz. At the same time, the harmonics at 3 GHz are suppressed by approximately 25 dB, while the harmonics at 7 GHz are suppressed by approximately 50 dB. Additionally, out-of-band suppression is found to be better than 20 dB over a wide frequency range for both the upper and lower sides of the filter. When the matched coplanar waveguides before and after are excluded, the area of the filter that is created when these targets are realized is 0.088λ x 0.095λ. This size results in a 7 times smaller filter than the one that the transceiver topology uses at the moment.

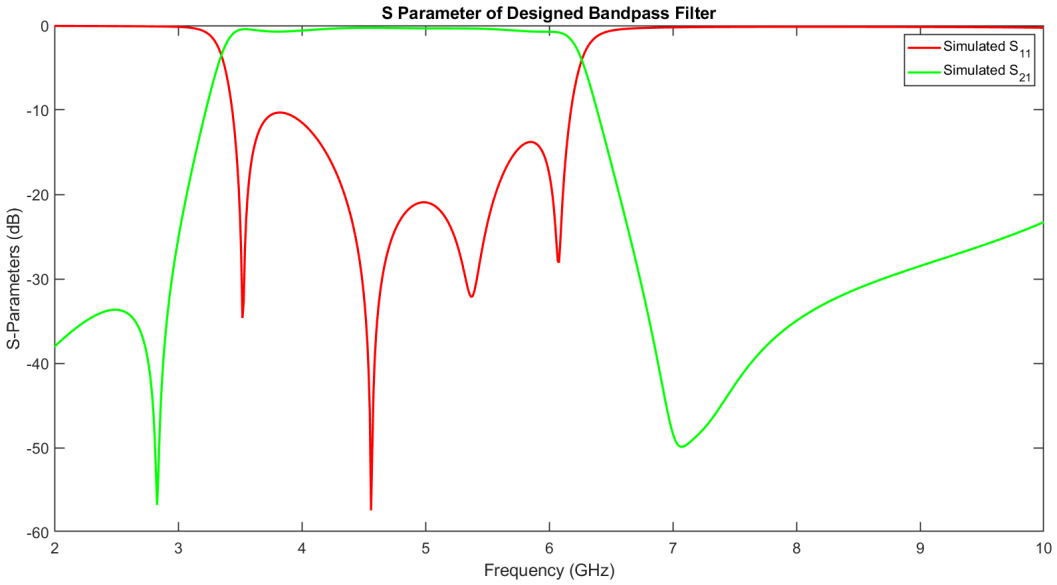


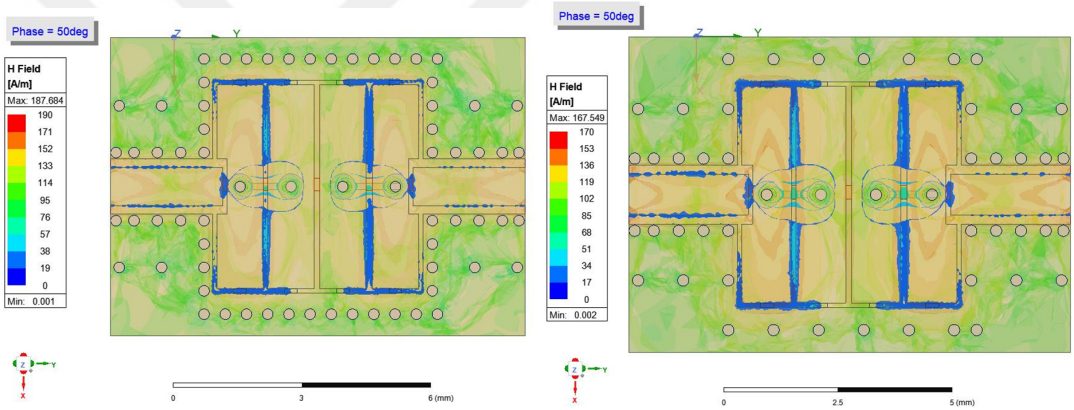
Figure 3.18: Simulation Result of Designed Bandpass Filter

The behavior of EM waves is investigated in order to assess the impact of the SIW structure on the bandpass filter through a variety of simulations. The first of the studies is to observe the shielding effect of the SIW structure. Initially, the designed filter is simulated using HFSS. The distribution of the electric field and magnetic field in the BPF between the input and output ports at 0° phase is monitored. Next, the same simulations are run again with half as many vias encircling the filter on both sides. It is observed that the shielding effect is reduced and EM waves leak through the vias as in Figure 3.19, and 3.20. Therefore, the radiation loss of the filter increases and the Q decreases. At the same time, this situation causes EMI formation.



(a) Ideal Shielding (b) Less Shielding

Figure 3.19: E-Field Distribution of Designed BPF



(a) Ideal Shielding (b) Less Shielding

Figure 3.20: H-Field Distribution of Designed BPF

In the second step, an analysis is conducted to see how the cavity structure of SIW affects the filter. This is accomplished by removing resonator patterns and vias at the top layer. Coplanar waveguide lines and external couplings at the input and output ports are kept the same. After that, the 3D structure seen in Figure 3.21 is created.

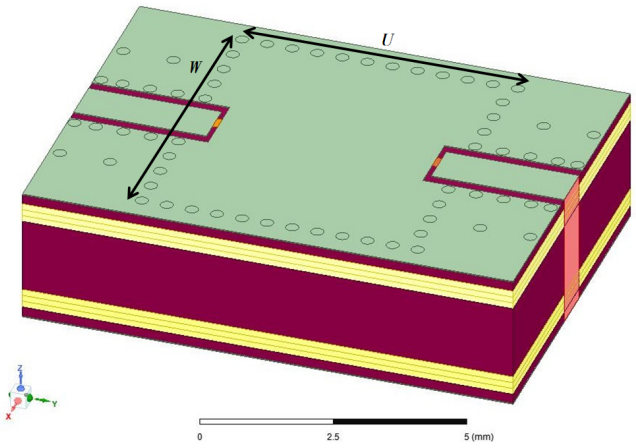


Figure 3.21: SIW Cavity Configuration

The 3D model is used to determine the length (U) and width (W) of the formed cavity. It is measured that the width and length are 6.25 mm and 5.63 mm, respectively. Following this, effective lengths are computed using Equations (2.33) and (2.36) with these values, as previously discussed in Chapter 2. The computations yield the following values: W_{eff} equals to 6.118×10^{-3} m, and U_{eff} equals to 5.498×10^{-3} m. Furthermore, Equation (2.38) is used to compute the resonant frequency using the obtained parameters. Consequently, a theoretical resonant frequency of 19.468 GHz is found. This calculation is further validated with HFSS simulations. Examining in Figure 3.22 reveals that the computed value has a minimum in S_{21} and a maximum in the S_{11} characteristic at the calculated resonant frequency.

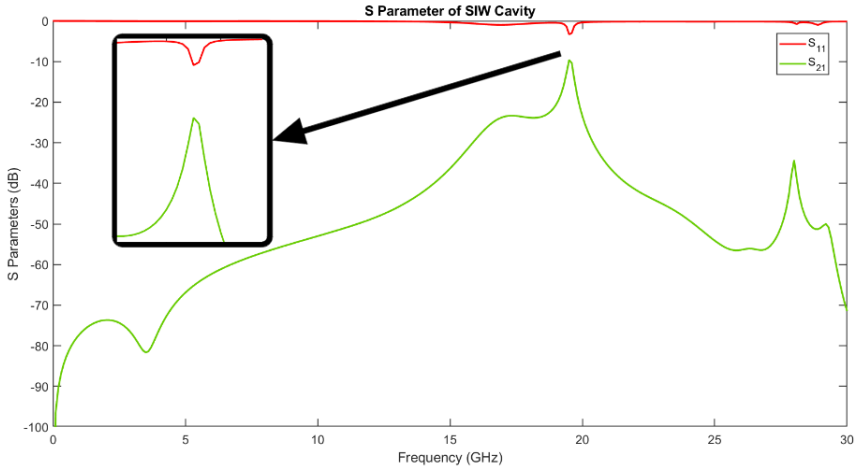


Figure 3.22: S Parameters of SIW Cavity

At this frequency, the propagation of EM waves is researched. It is verified that there is signal transmission at the detected frequency by observing the E-field distribution of the constructed cavity structure as shown in Figure 3.23. Since the resonant frequency is far from the passband frequencies of the proposed filter, the filter characteristic is not affected by the cavity.

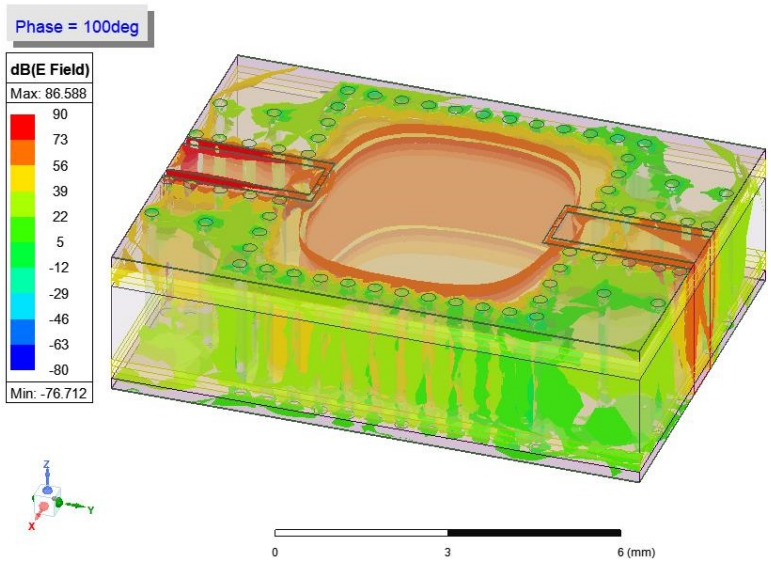


Figure 3.23: E Filed Distribution of SIW Cavity

3.7 Circuit Representation

Figure 3.24 displays the circuit schematic of the 4th-order filter that is presented in [38]. The total of the lumped and distributed capacitances between the resonators and coplanar waveguides forms the C_{S1} and C_{S5} capacitors. The combination of the capacitance created by the space between the resonators and lumped capacitances is represented by the other series-connected capacitances (C_{S2}, C_{S3}, C_{S4}). A short circuit line pattern formed on the intermediate layer yields the L_{S1} and L_{S2} inductors. Four parallel resonator circuits are also connected to the ground. Using Equation (3.1), the inductance value for the vias in the resonators can be determined. Once more, the distributed capacitance between the ground and the conductor patches, as well as the lumped parts, contributes to the capacitance value of resonators. In addition, since the filter is symmetrical, there are circuit elements equal to each other.

The equivalent components are as follows: $C_{S1} = C_{S5}$, $C_{S2} = C_{S4}$, $L_{S1} = L_{S2}$, $C_{P1} = C_{P4}$, $C_{P2} = C_{P3}$, $L_{P1} = L_{P2} = L_{P3} = L_{P4}$.

The TZ position that establishes the lower cutoff frequency is altered by the C_{S3} value. Pairs C_{S2} and L_{S1} as well as C_{S4} and L_{S2} identify the TZs that establish the higher cutoff frequency. C_{S1} and C_{S5} define the input and output coupling.

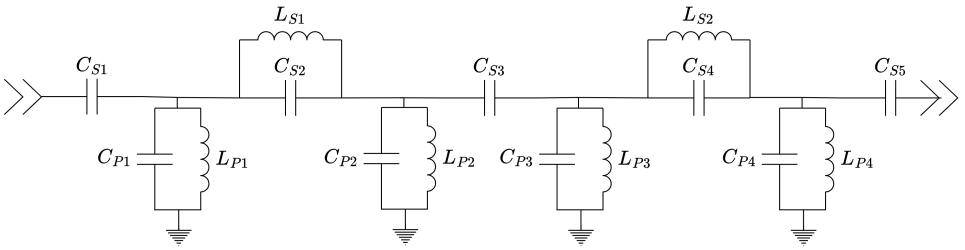


Figure 3.24: Circuit Representation of Bandpass Filter

It is discovered throughout the investigations that this circuit model is not adequate for a design application. The first major deficiency is specifically the absence of a clear link about how the values of the elements are established. To be more specific, the amount to which distributed elements contribute to lumped elements is unknown. Furthermore, there is a discrepancy between the circuit representation and the actual physical patterns of the filter design. This situation leads to inconsistencies between EM and circuit simulation. For example, when the layer where the short circuit line is located is altered, the circuit response and EM simulation do not behave the same way.

Because of the aforementioned reasons, an improved circuit representation is proposed in this study. It is aimed to facilitate filter design by increasing its agreement with EM simulations. The proposed circuit represents the behavior of the filter better than the first version. Thus, the effects of variables can be observed in a time-efficient and resource-efficient manner without the need for long simulations at the initial stage of the design. Since the connection between the values of the elements in the proposed circuit and their physical counterparts are established in detail, the designer can make bidirectional use from the model to the circuit or from the circuit to the model. In this way, the circuit can be used not only at the first stages of the design but also in the fine-tuning phase.

The developed circuit diagram is displayed in Figure 3.25. There are two important modifications made to the circuit. The first of these is to separate the L_{P1} value, which represents the total through via inductance in the old circuit, as two serial inductors (L_{P1} and L_{P2}) from the point where the short circuit line is connected in the new circuit. The ability to demonstrate the shifting position impact of the short circuit line pattern is the primary motivation for this. The second change is the addition of capacitors parallel to the separated inductors. In this manner, the capacitances between the ground and the short circuit line (C_{SG}) and between the patch resonators and the short circuit line (C_{PS}) are expressed individually. Lastly, the capacitance of the resonators with the ground around them and at the bottom layer is represented by C_{P1} and C_{P2} capacitances.

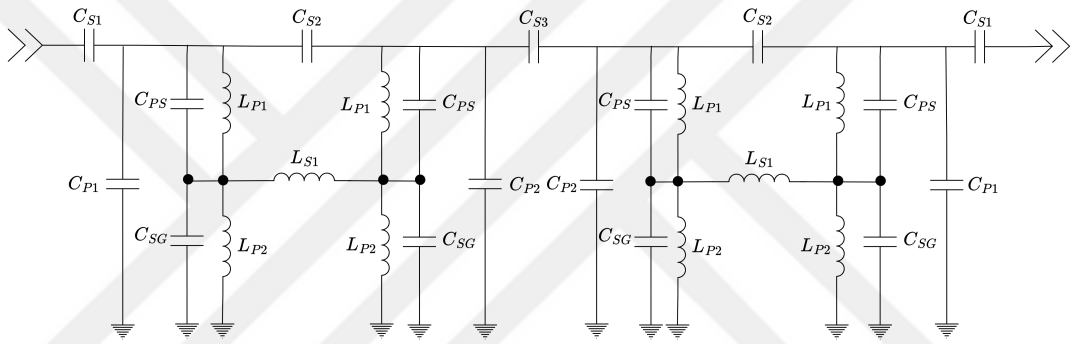
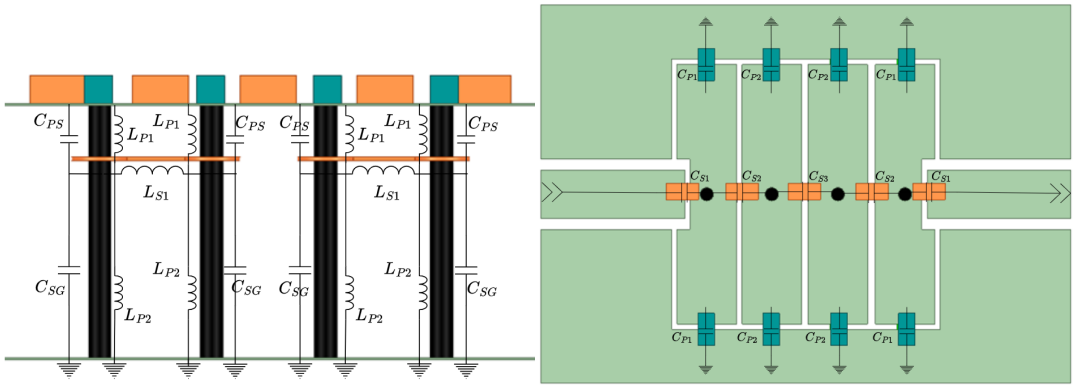


Figure 3.25: Improved Circuit Representation of Bandpass Filter

Figure 3.26 shows the physical equivalent of each circuit element in the proposed circuit model. Dielectric layers of the PCB and shielding ground vias are hidden for clear demonstration. The capacitances between the resonator plates and the bottom ground layer are also added to the C_{P1} and C_{P2} capacitance calculations besides the elements seen in the figure.



(a) Short Circuit Line Related Components (b) Resonator Related Components

Figure 3.26: Physical Counterparts of Circuit Elements in Improved Circuit Model

Providing an expanded description of how these circuit elements can be retrieved from physical factors is another significant enhancement to schematics. Q3D is used to simulate inductance values of via and short circuit line drawings [57]. Figure 3.27 shows the frequency-dependent inductance change of the 2.746 mm long via used in the design. Then, the through via inductance of 1.565 nH is proportioned according to the layer of the short circuit line pattern. The values of L_{P1} and L_{P2} are computed as 0.348 nH and 1.217 nH respectively, taking into account the 0.611 mm distance between the top layer and the short circuit line.

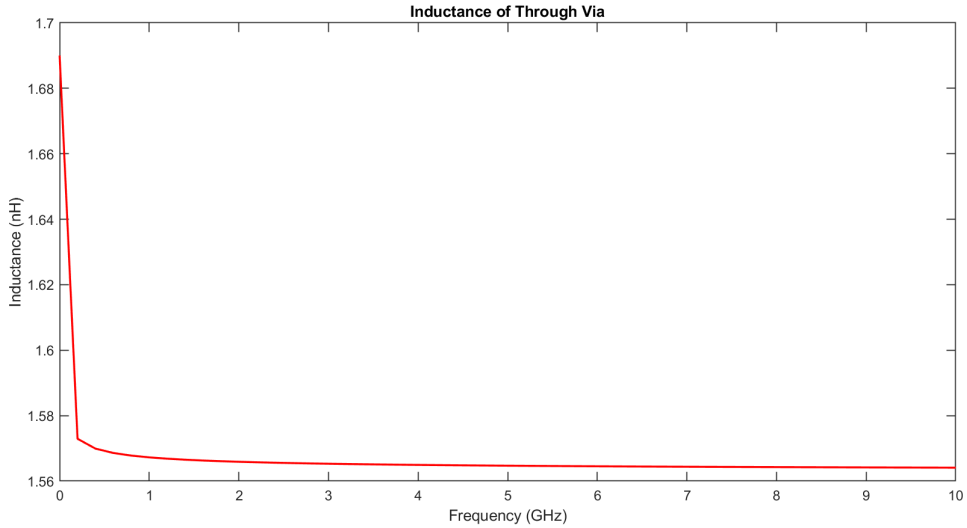


Figure 3.27: Inductance of Through Via Used in Designed Filter

The identical Q3D simulation is performed using the short circuit line topology shown in Figure 3.28 and its 130 µm upward shift. Simulation results are shown in Figure 3.29. After the L_{P1} value is found as 0.348 nH, it is subtracted from the inductance of the overall short circuit line structure which is found as 0.852 nH. The residual inductance value solely indicates the inductance of the line pattern or the L_{S1} value as 0.156 nH for the lower layer positioned short circuit line.

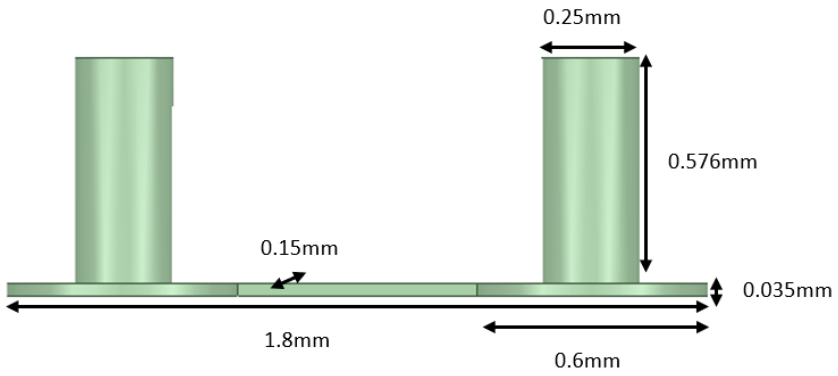


Figure 3.28: Short Circuit Line Pattern in Designed Filter

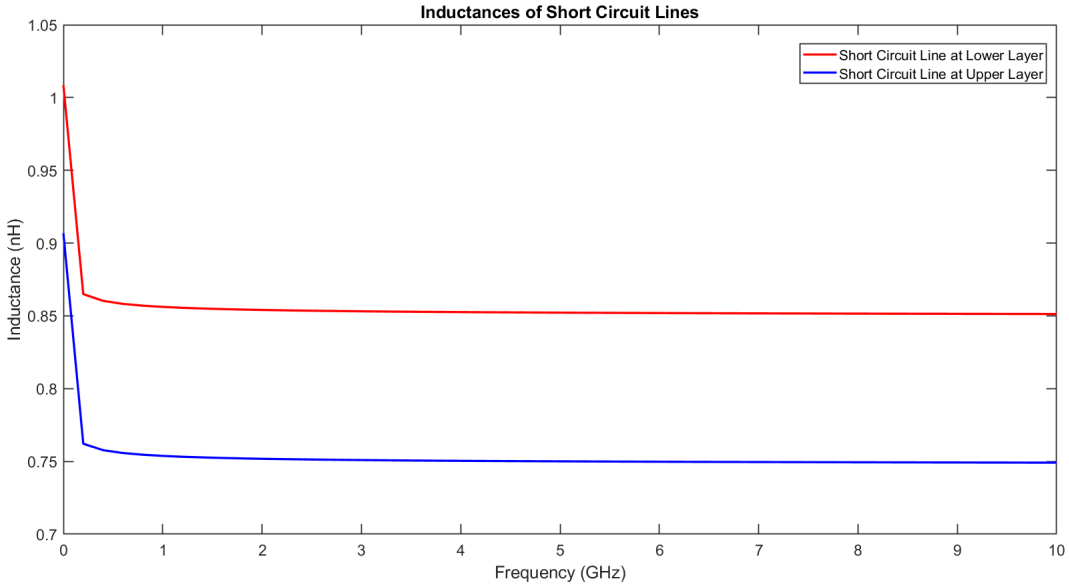


Figure 3.29: Inductance of Short Circuit Line Used in Designed Filter

For the version where the short circuit line is relocated on the upper layer by 130 µm, all inductance calculations are repeated. The inductance values for L_{P1}, and L_{P2} are calculated as 0.274 nH, and 1.291 nH respectively. Then, the 0.202 nH inductance

value of the pattern in the intermediate layer, i.e. L_{S1} is obtained by deducting the L_{P1} value from the 0.75 nH inductance value of the whole short circuit line.

The contribution of distributed coupling capacitance and lumped capacitance values are two significant aspects taken into account when evaluating the values of serial capacitances. Equation (3.21) is used for the distributed capacitance calculations of the resonators [71]. The dielectric constant in Equation (3.21) can be found with the multiplication of absolute permittivity (ϵ_0) and relative permittivity (ϵ_r). Also, W_R represents the conductor width, L_R stands for the conductor length, and d represents the distance between them.

$$C_{Sdist} = \epsilon_r \epsilon_0 \frac{1}{\pi} W_R ln\left(1 + \frac{2L_R}{d_R}\right) \tag{3.21}$$

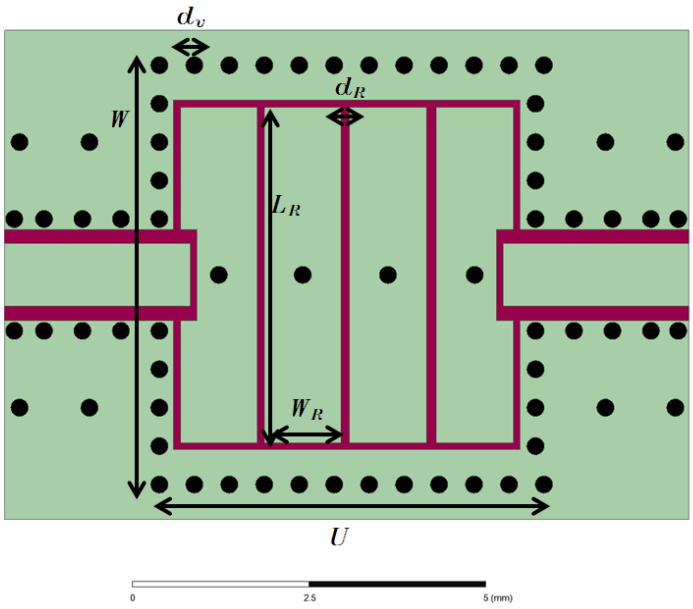


Figure 3.30: Dimension Parameters of BPF Design

As the resonator patches are positioned on the uppermost layer in the design, a portion of the electric field propagates through the air. For this reason, the effect of air and ϵ_r should be considered together. Equation (3.22) or Equation (3.23) should be used depending on the ratio of the width of the conductor to the thickness of the PCB (l) [72].

When $\frac{W_R}{l} < 1$

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2}\left[\left(1 + 12\frac{l}{W_R}\right)^{-1/2} + 0.04\left(1 - \frac{W_R}{l}\right)^2\right] \tag{3.22}$$

When $\frac{W_R}{l} \geq 1$

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2}\left(1 + 12\frac{l}{W_R}\right)^{-1/2} \tag{3.23}$$

The effective dielectric constant is calculated using the given Equation (3.22) since $\frac{W_R}{l}$ rate is smaller than 1 in this design. The result is found to be 2.523 by utilizing ϵ_r as 3.55, l as 2.746 mm, and W_R as 1.1 mm. After that, C_{Sdist} capacitance is obtained as 0.036 pF by implementing d_R as 0.1 mm, L_R as 4.8 mm, and other previously mentioned values. The fact that the resulting capacitance value is much smaller than the lumped ones has led to the determination that the lumped element values are much more dominant than the distributed ones for serial capacitances. Then, acquired distributed coupling capacitances are added to the lumped ones to obtain series capacitance values, as given in Equation (3.24).

$$C_S = C_{Sdist} + C_{Slumped} \tag{3.24}$$

The parallel plate capacitances C_{SG} and C_{PS} are calculated using the Q3D simulation. The same simulation is repeated when the short circuit line is moved to the upper layer. As anticipated, there is a slight increase in the C_{PS} capacitance and a drop in the C_{SG} capacitance in the second scenario.

Finally, C_P values are obtained by adding distributed and lumped values, according to Equation (3.25). The values of $C_{Plumped}$ are chosen to be 0.2 pF for every resonator. To extract the value corresponding to C_{Pdist} from the 3D model, multiple studies need to be conducted in parallel.

$$C_P = C_{Pdist} + C_{Plumped} \tag{3.25}$$

When evaluating distributed capacitance, a Q3D model is typically preferred. However, using only Q3D would be incomplete in this study. The reason behind this is

that Q3D computes the capacitance value by electrostatic calculations. Consequently, it is thought that there is an equal distribution of electric charges throughout the conductor and the voltage is constant for the conductor assigned as signal. In addition, no physical connection between the conductor defined as ground and the conductor identified as signal is accepted by the Q3D tool in order to run the simulation. This means that the design must be modified to remove the shorting vias that make up the resonator structure. These factors lead to the implementation of full-wave analysis in HFSS simulation to account for the impact of the nonuniform distribution of the electric field in the computations. The E-field change for each of the four resonators on the model is measured at certain marker points with varying phases, as Figure 3.31 illustrates.

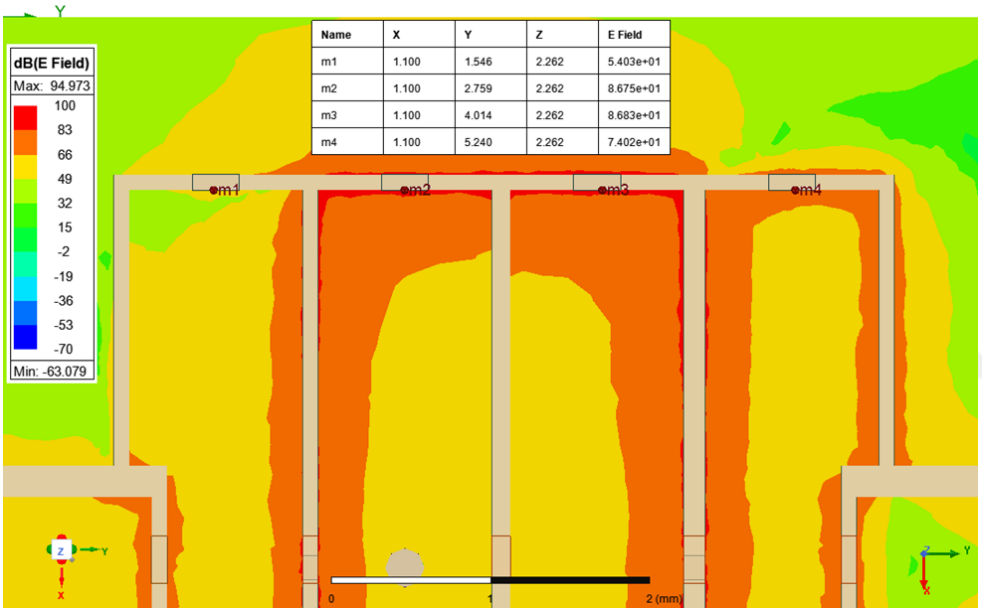


Figure 3.31: E-Field Measurements for Phase 130°

Table 3.3 presents an overview of the data that are acquired from these measurements. The average E-field values, expressed in dB, considering 18 distinct phases are listed in Table 3.3. The investigation yielded a ratio of 1.49 between the E-fields of the second & third resonators and the first & fourth resonators.

Table 3.3: E-Field Measurements of Resonators in BPF

Phase (degree)	M1 (dB)	M2 (dB)	M3 (dB)	M4 (dB)
0	79.46	83.17	82.34	78.86
10	80.60	82.92	81.43	78.99
20	81.37	80.69	78.48	80.56
30	81.83	77.29	73.53	81.66
40	82.02	71.13	59.55	82.40
50	81.93	47.28	69.18	82.83
60	81.58	72.16	76.41	82.98
70	80.93	77.79	80.13	82.87
80	79.94	81.00	82.53	82.49
90	78.52	83.13	84.19	81.81
100	76.49	84.63	85.36	80.78
110	73.47	85.67	86.15	79.30
120	68.36	86.36	86.63	77.19
130	54.03	86.75	86.83	74.02
140	65.09	86.87	86.76	68.49
150	71.88	86.72	86.42	46.59
160	75.49	86.29	85.79	67.00
170	77.83	85.56	84.82	73.30
Average	76.15667	80.30056	80.91833	76.78444

In order to find the relationship between the electric field and capacitance, two equations must be taken into account. The energy stored in the capacitor (U_{cap}) is expressed in the E-field-based formulation shown in Equation (3.26) based on. In Equation (3.27), the same stored energy is calculated with capacitance (C) and voltage (V). For constant V, there is a direct proportion between C and E^2. For this reason, when calculating the capacitance in the 2nd and 3rd resonators, the distributed capacitance value obtained from Q3D simulations should be multiplied by the square of the E-field ratio.

$$U_{cap} = \frac{1}{2}\epsilon \int |E|^2 \, dV \tag{3.26}$$

$$U_{cap} = \frac{1}{2}CV^2 \tag{3.27}$$

The Q3D capacitances are obtained as 0.34 pF and 0.21 pF for C_{P1dist} and C_{P2dist} respectively. The 0.34 pF value is used directly for C_{P1dist}. After the addition of $C_{P1lumped}$ value which is 0.2 pF, the C_{P1} value is obtained as 0.54 pF. On the other hand, the square of the 1.49 ratio that comes from the full wave analysis is multiplied by 0.21 pF for the exact value of C_{P2dist}. Then, by adding $C_{P2lumped}$ value as 0.2 pF, 0.66 pF is obtained for C_{P2} value.

Table 3.4 provides the values of the proposed circuit elements utilized for two distinct short circuit line positions. The calculated equivalent value is not exact only for C_{P2}. The circuit simulation is done by decreasing the C_{P2} value by 0.02 pF.

Table 3.4: Resultant Values of Improved Circuit Components

Short Circuit Line Position	Lower Layer	Upper Layer
C_{S1}	0.98 pF	0.98 pF
C_{S2}	0.33 pF	0.33 pF
C_{S3}	0.53 pF	0.53 pF
C_{P1}	0.54 pF	0.54 pF
C_{P2}	0.64 pF	0.64 pF
C_{PS}	0.1 pF	0.13 pF
C_{SG}	0.09 pF	0.06 pF
L_{P1}	0.348 nH	0.274 nH
L_{P2}	1.217 nH	1.291 nH
L_{S1}	0.156 nH	0.202 nH

On the other hand, Table 3.5 shows the values used to simulate the initial state of the circuit. As explained before, through-via and short-line inductance values are taken as the values found for the entire structure. Series capacitance values are the same as the values in the proposed circuit. The values that provide the closest results to the simulation result are placed as parallel capacitance values.

Table 3.5: Resultant Values of Initial Circuit Components

Short Circuit Line Position	Lower Layer	Upper Layer
C_{S1}	0.98 pF	0.98 pF
C_{S2}	0.33 pF	0.33 pF
C_{S3}	0.53 pF	0.53 pF
C_{P1}	0.56 pF	0.56 pF
C_{P2}	0.61 pF	0.61 pF
L_{P1}	1.56 nH	1.56 nH
L_{S1}	0.852 nH	0.75 nH

In order to demonstrate the detected inconsistency of the initial circuit model, a filter simulation is made with the short circuit lines in both their own layer and upper layer. Then, the results are compared with the circuit response. As can be seen in Table 3.5, only L_{S1} values in the circuit are changed according to the Q3D simulation results in order to reflect the change in the layout. Figures 3.32 and 3.33 display the significant variation in the outcomes.

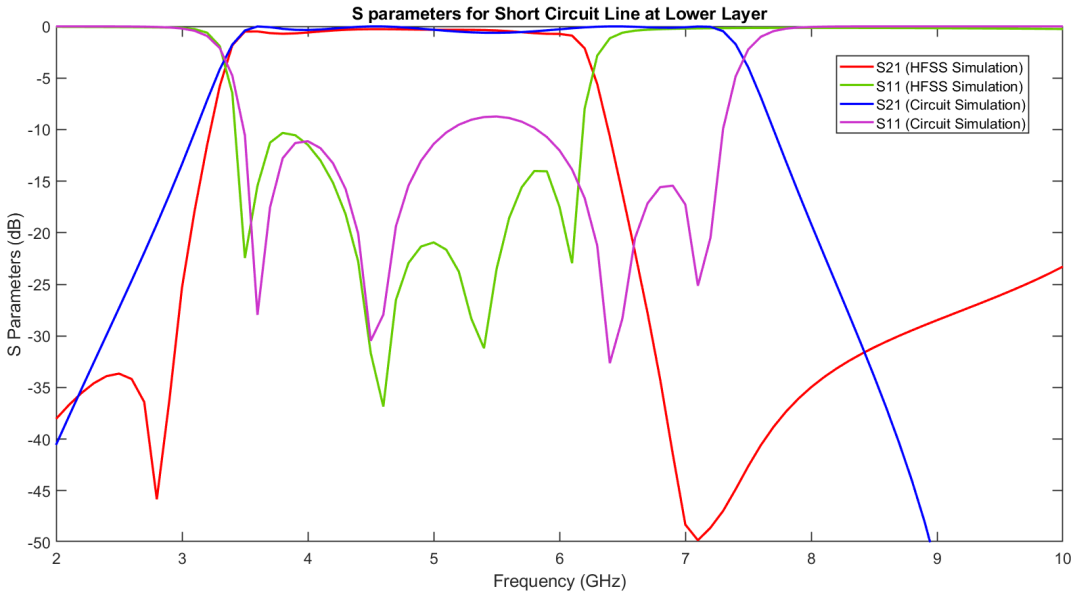


Figure 3.32: S parameters for Short Circuit Line at Lower Layer

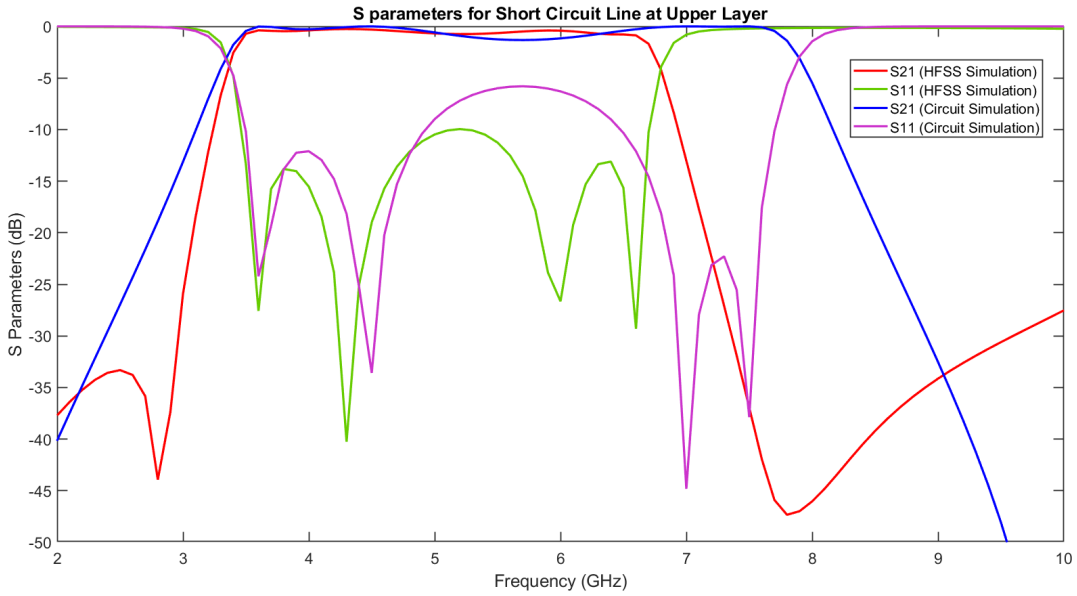


Figure 3.33: S parameters for Short Circuit Line at Upper Layer

Furthermore, the 3D model simulation and improved circuit results, when the short circuit line is in its position, are compared in Figure 3.34. A similar comparison is made for the scenario where the short circuit line is positioned in the upper layer in the other Figure 3.35.

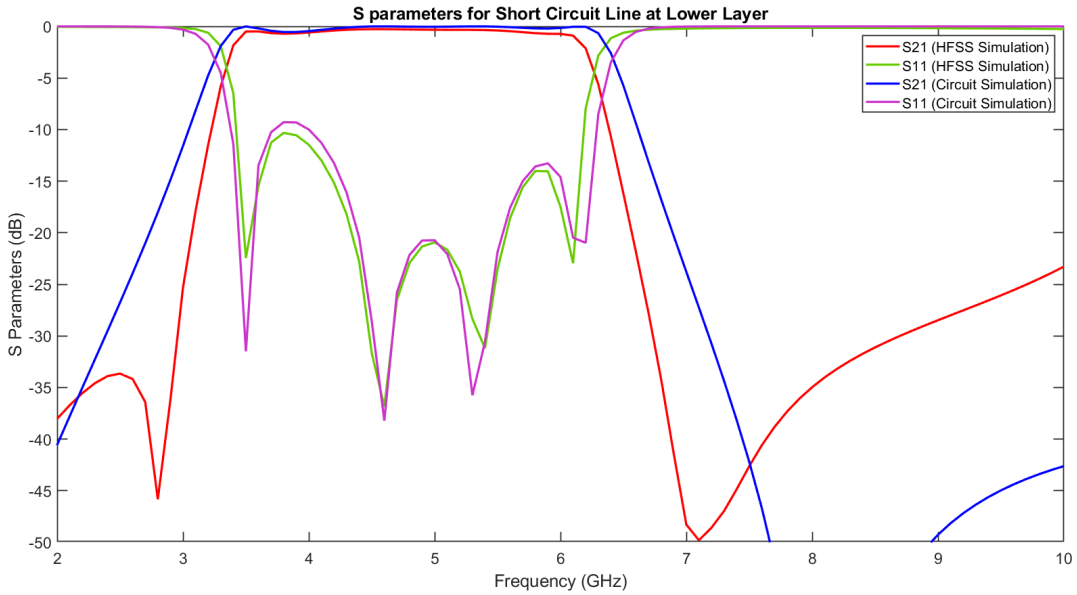


Figure 3.34: S parameters for Short Circuit Line at Lower Layer

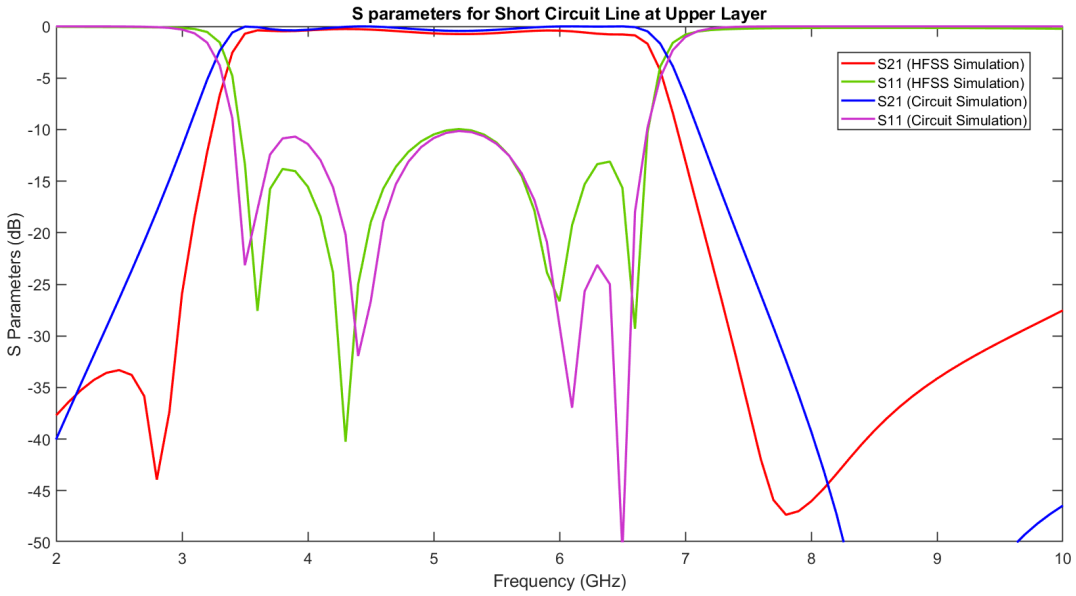


Figure 3.35: S parameters for Short Circuit Line at Upper Layer

The agreement of the two circuits with the 3D model simulation, changing layout, and stack-up properties are compared. For the initial circuit diagram, a significant variation in the passband is seen when related Figure 3.32 and 3.33 are examined. Particularly at the higher cutoffs, there is a considerable difference when the circuit response is obtained with acceptable component values. The locations of reflection zeros (RZ) vary greatly as well. On the other hand, the present enhanced circuit essentially complies with the HFSS model simulation and exhibits negligible cut-off changes and RZ positions. Moreover, analytical and computational explanations are provided for how the values of every circuit element are determined.

3.8 Particle Swarm Optimization to Verify Filter Optimality

The designer must perform many parametric analyses to create the filter that provides the desired specifications, as explained in Section 3.4. These analyses are simulation-based and are carried out using HFSS. Because of the comprehensive consideration of EM wave behavior in the HFSS, optimized values for the designs are provided with greater accuracy. However, this method is also computationally expensive. For this reason, these analyses require a lot of time and power to provide component values.

On the other hand, MATLAB can speed up the selection of parameter values if the structure can be represented by a circuit model. This is demonstrated by the research on ground capacitance values selection in this study, which optimizes the S_{11} characteristic of the filter. Out of all the optimization techniques, PSO is selected because of its many advantages. The first advantage is that compared to GA or DE approaches, it is simpler to apply. Secondly, since it performs a global search, the probability of finding the local optimum is lower [51]. Its ability to quickly and reliably converge to a result is another factor. Additionally, it can be applied to nonlinear or noncontinuous functions; in this study, the nonlinear S_{11} function will be the function of interest. It also searches for the optimum solution without requiring gradient information, which is advantageous for an examination of EM simulations. Other details about the PSO technique are given in the Appendix A.

The algorithm in Figure 3.36 is created for this study to optimize the S_{11} value by changing the C_p capacitances as variables. The upper boundary is specified as 10 dB for the magnitude of S_{11} in the objective function. Then, the penalty is calculated using formulation in Equation (3.28).

$$penalty = sum((s11_{mag} > 10^{upperBound/20}) \times (s11_{mag} - 10^{upperBound/20})^2) \quad (3.28)$$

Moreover, the sum of the penalties is minimized by assigning it to the objective value. The solution space is set by defining upper and lower boundaries to be tested as capacitance.

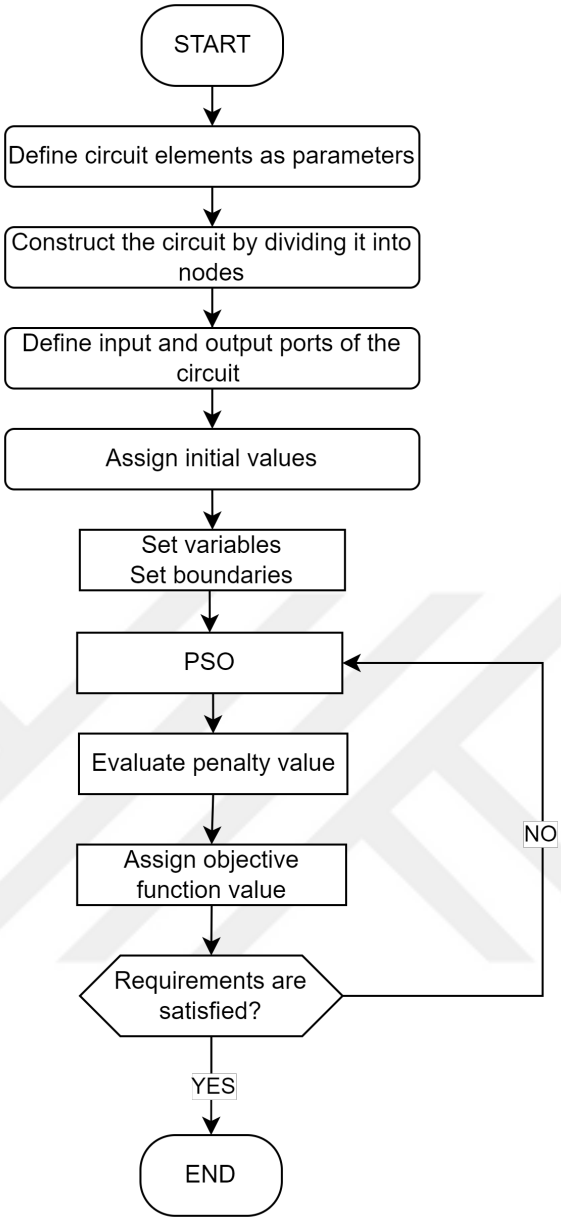


Figure 3.36: Flow Chart of the Optimization Algorithm for BPF Design

The required parameters are provided to the particle swarm function for optimization, including the objective function, number of variables, boundaries, swarm size, maximum iterations, etc. The summary of them can be seen in Table 3.6.

Table 3.6: PSO Parameters

Swarm Size	100
Max Iterations	100
Max Stall Iterations	20
Inertia Weight	[0.4, 0.9]
Cognitive Coefficient	1.49
Social Coefficient	1.49

Figure 3.37 illustrates that the inertia weight is a linearly decreasing function. It is possible to search for the ideal values of capacitances throughout an extensive area of the solution space by starting the optimization with the largest inertia weight.

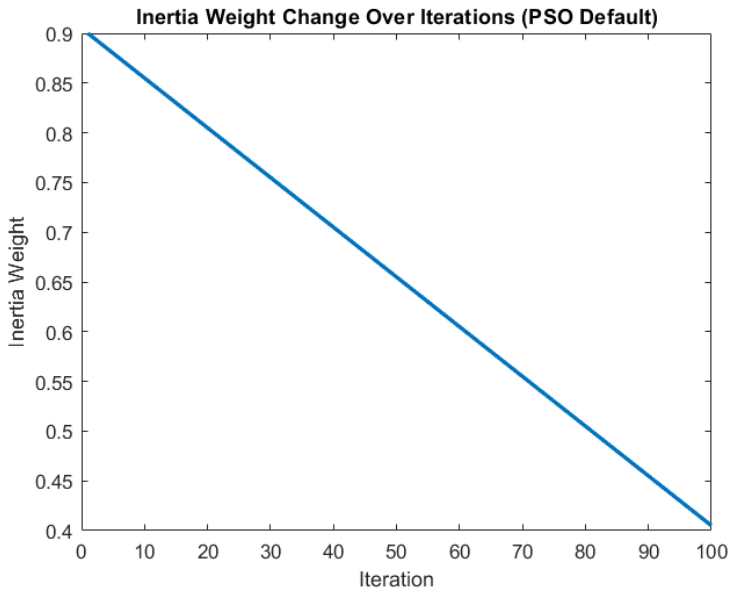


Figure 3.37: Inertia Weight Change Over Iterations

Capacitance values that can be placed with a resolution of 0.05 pF are obtained as in real life with Equation (3.29), where distributed values are denoted as $distVal$ and optimized values are demoted as $optVal$. Finally, the S parameter of the optimized circuit is obtained by using the latest optimized values.

$$optVal = round\left(\frac{optVal - distVal}{0.05 \times 10^{-12}}\right) \times 0.05 \times 10^{-12} + distVal \qquad (3.29)$$

Only the distributed parts of C_P values are used to obtain the S parameters in Figure 3.38 once the algorithm is built. These are 0.34 pF and 0.44 pF for C_{P1} and C_{P2} respectively. Other circuit elements are assigned as shown in Table 3.4 obtained while creating the circuit model.

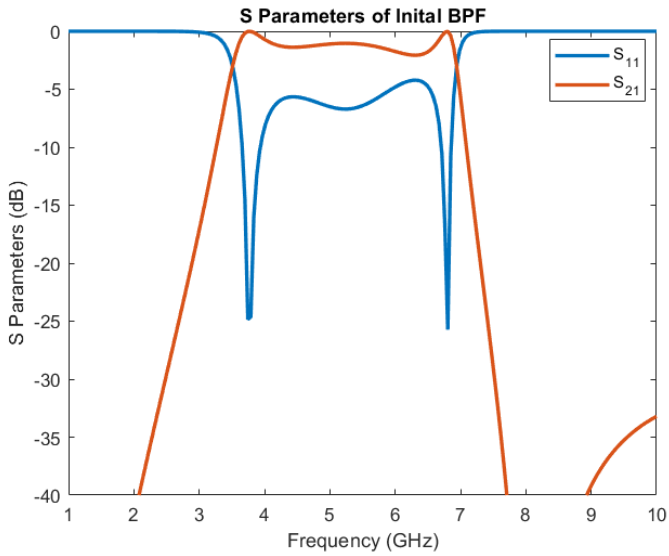


Figure 3.38: S Parameters of Initial BPF

Then, C_P values are updated according to the PSO, and the objective value is minimized to finalize the optimization process as in Figure 3.39. The best function value is obtained as 0.139424.

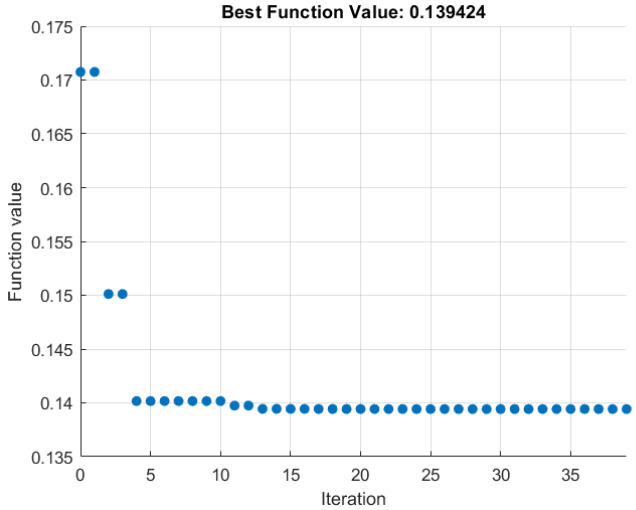
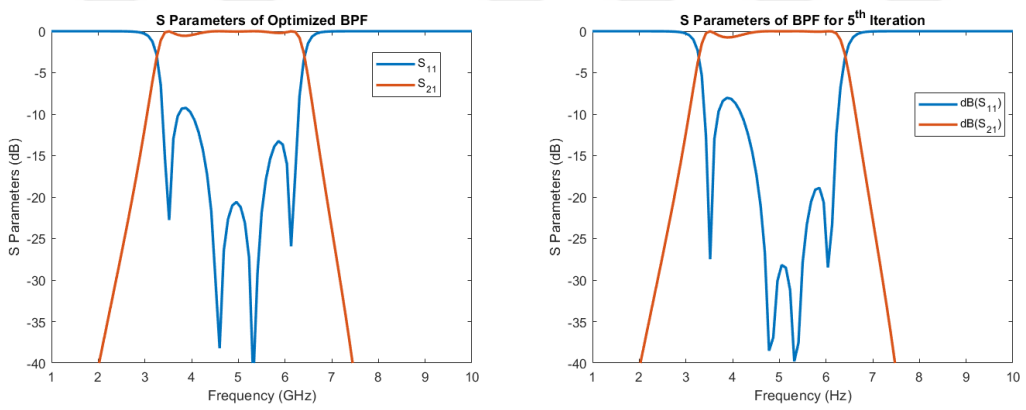


Figure 3.39: Function Value for Each Iteration

Following optimization, C_{P1} and C_{P2} have values of 0.54 and 0.64 pF. As a result, the filter designed using EM simulations and the filter designed with MATLAB are exactly the same. The optimized filter result is shown in Figure 3.40a. Additionally, the process requires only two minutes and twenty seconds to accomplish this outcome.

After the fifth iteration, no noticeable variance is identified when the best function value change is examined. Because of that, the filter characteristic that can be achieved by establishing a maximum of five iterations is observed. As a result, the capacitance values and the frequency response of the filter are generated very close to the optimum response following the designated iteration. Figure 3.40b illustrates the slight change in frequency response due to the increase in the best function value from 0.139424 to 0.140229. The optimization time is thereby lowered to 24 seconds.



(a) S Parameters of Optimized BPF

(b) S Parameters of BPF for 5^{th} Iteration

Figure 3.40: S Parameters of BPF Design for Different Iterations

3.9 Manufacturing Process

The design dimensions and lumped capacitance values for the bandpass filter are determined based on iterative simulations. After that, the layout of the BPF is created using the Mentor Pads tool. The compliance of the design with the manufacturing limits is double-checked during the drawing process. For example, the vias that comprise the walls of the SIW structure are examined again since the minimum distance between two holes on the board must be 4 mils. Another example is that 4 mils is

specified as the minimum value for the width of the lines in the 35-micrometer copper interlayer. This leads to another confirmation of the short circuit line widths. The solder mask on the surface is removed in the necessary areas so that the lumped capacitors and the appropriate connector can be soldered to the PCB. Surface mount type stainless steel SubMiniature Push-on (SMP) connector is chosen as the connector for the filter. One benefit of this connector is that, regardless of the thickness of the PCB, it can be soldered if the proper board outline modifications are made on the edge. Additionally, it has a small size that does not enlarge the already small size of the filter and an IL of approximately 0.12 dB between 0 and 18 GHz. Considering the pin length of the SMP, the coplanar line length at the filter input and output is determined. An image of the SMP connector used in the filter is shown in Figure 3.41.



Figure 3.41: SMP Connector

As lumped capacitance, the 0201 packaged capacitor series of the Murata is used. These particular capacitor series have a rated voltage of 50 V. This resulted in the creation of the layout drawing seen in Figure 3.42. A through line is inserted adjacent to the filter layout in order to test the connector, matched coupled line, and set up.

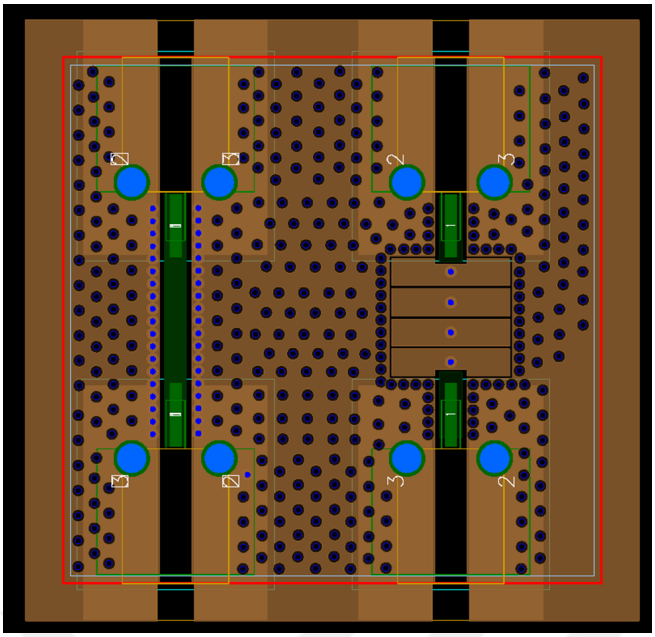


Figure 3.42: Layout of Designed BPF

The consistency of the measurement results is verified by manufacturing a number of PCBs, soldering the elements on them, and measuring them. The photo of the first prototype, whose manufacturing and assembly are completed, can be seen in Figure 3.43.

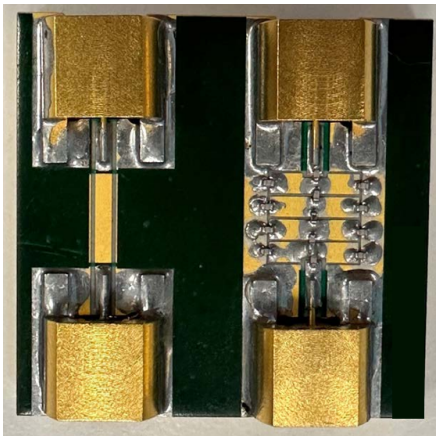


Figure 3.43: Manufacturing Result of Designed BPF

3.10 Measurement Setup and Results

The post-manufacturing tests are conducted using the Rohde & Schwarz ZNA43 Vector Network Analyzer, which is seen in Figure 3.44. The operating frequency range of the gadget is 10 MHz - 43 GHz. The remote control feature allows for the transfer of measurement data files after the measurements are completed, and the predetermined performance specifications are used to evaluate the findings.

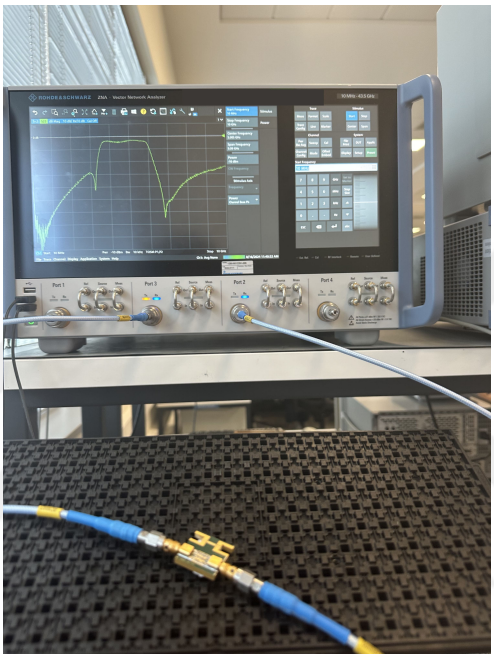


Figure 3.44: Measurement Setup

The completed design simulation and the post-manufacturing measurement results are contrasted in Figure 3.45. The differences between simulation and manufacturing results can be caused by multiple causes. The first reason for this may be the tolerances in the gap around the resonator structures and coplanar line during manufacturing. Likewise, errors that may change the width or length of the short circuit line in the intermediate layer change the characteristic. The imperfection of the RF SMP connectors and lumped capacitors is another factor. Lastly, these variations can have resulted from variations in the thickness of the materials employed in the stack-up during manufacturing.

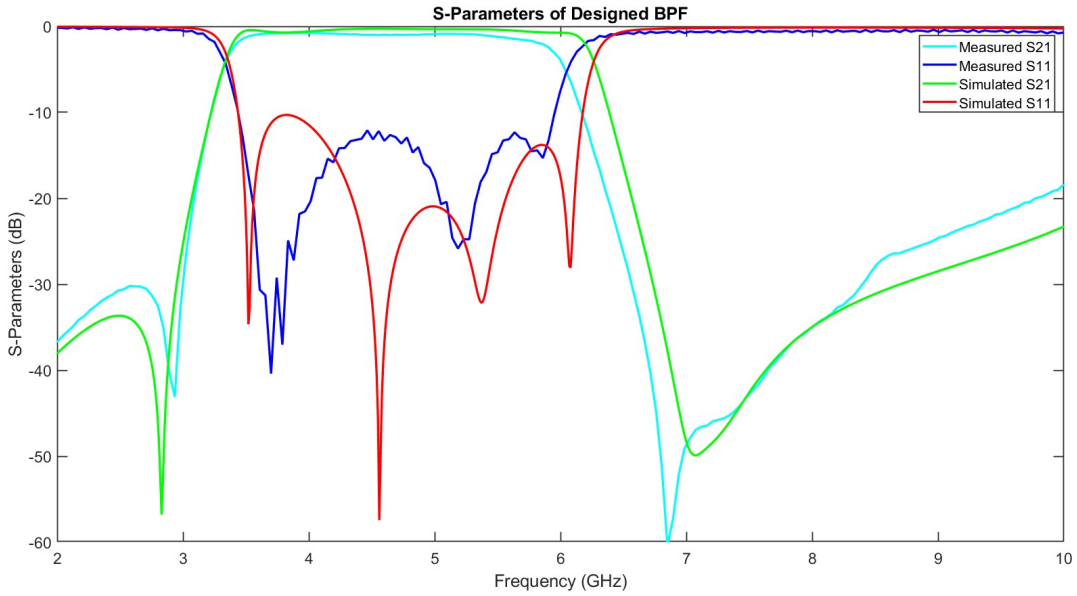


Figure 3.45: Simulation and Measurement Results of Designed BPF

Particularly the difference in the high cutoff frequency of the filter is observed in Figure 3.45. The possibility that capacitance tolerance is the cause of the variation in the outcome is assessed. For this purpose, the capacitance employed as C_{S2}, which influences the high cutoff, is found to have a tolerance of $\pm$ 0.1 pF. A parametric sweep simulation of the capacitance is performed with 0.05 pF steps. Simulation and measurement results are combined in Figure 3.46. The simulation with a 0.35 pF capacitance and the experimental data overlapped, as the Figure illustrates. Hence, it is verified that capacitor tolerance accounts for the discrepancy between design and manufacturing outcomes.

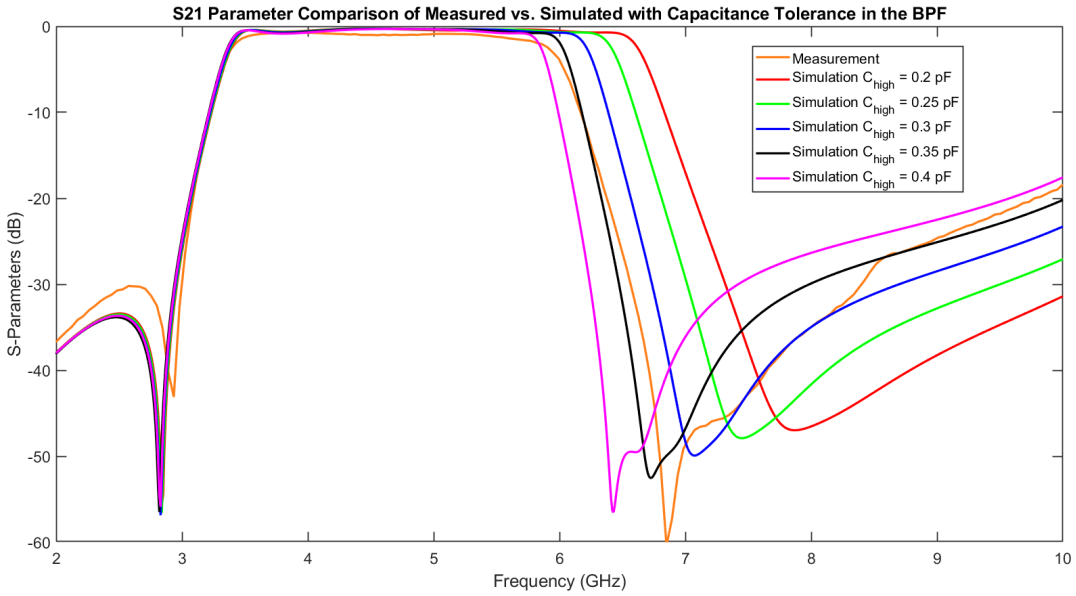


Figure 3.46: S_{21} Parameter Comparison of Measured vs. Simulated with Capacitance Tolerance in the BPF

Variations in the S_{11} parameter could be caused by multiple factors. While one of the possible reasons is the changes in the cutoff frequency, another reason is the tolerances in the ground capacitance values. Hence, no additional research is carried out to identify precisely corresponding capacitance values for the post-manufacturing S_{11} curve.

CHAPTER 4

TUNABLE SIW BANDPASS FILTER DESIGN

Although the BPF, whose design is described in Chapter 3, is achieved to meet the design specifications, some drawbacks are identified. The first is that the capacitors need to be altered and soldered again if different adjustments are desired for the manufacturing output. Since the size of the elements is 0201 packages, this process is not very easy. At the same time, since the values of the commercially available lumped capacitors are fixed, the resolution with which the filter characteristic can be changed is limited. For these reasons, there is a need to change the capacitance values without any manual intervention and to do this at a higher resolution. As a solution, extensive research is carried out to turn the filter into a tunable one.

4.1 Tuning Mechanism Determination

An RF filter can be made adjustable in a number of ways. The first technique that might be used would be the technology known as MEMS. These small mechanical mechanisms that adapt to changing electrical impulses are used to produce switching in designed filters [2]. The next technique is utilizing piezoelectric materials. Different mechanical characteristics are displayed by these materials as the electric field changes [73]. As an alternative, an external magnetic field can be used to adjust the resonant frequencies, or magnetic alignment, of ferromagnetic materials [74]. Ferroelectric materials can be employed as tuning elements because an externally applied electric field can alter the electric polarization properties [74]. Another strategy is to use semiconductors such as pin or varactor diode. When used as a switch or variable resistor, PIN diodes are the recommended option. A varactor diode is a good

choice when a variable capacitor is required. In PIN diodes, there is an intrinsic layer between the p-type and n-type layers. This intermediate layer acts as conductive or resistive depending on whether the diode is forward or reverse-biased. Varactor diodes are p-n junction diodes and are always operated in a reverse bias state. Depending on the applied voltage magnitude, the capacitive effect of the element changes because of the change in the depletion region size [2].

The most important reason for choosing the varactor diode technique as the tuning method for this design is that it has a wide tuning range in a very small size. For this reason, it is a highly preferred component in wideband filter designs. Furthermore, while ferromagnetic materials, MEMS, ferroelectric, and other tuning approaches are more costly, complex, and have a high power consumption. On the other hand, varactor diode technology is a suitable choice since it is inexpensive, user-friendly, and efficient with nearly negligible power consumption [2]. Other details about the structure and operating principles of the varactor diode are given in the Appendix B.

The equivalent circuit for the varactor diode is shown in Figure 4.1. As can be seen in the circuit, there is the depletion layer capacitance C_j and the resistance R_s caused by the bulk, leads, and contacts. Both of these terms have a voltage-dependent function. This is how the tuning ability of the varactor diode occurs. Additionally, there are some elements with fixed values in the circuit. $C_{parasitic}$ symbolizes case capacitance and L_s symbolizes lead inductance.

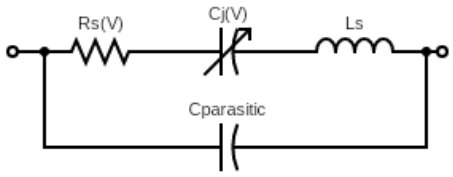


Figure 4.1: Equivalent Circuit of Varactor Diode

Depending on the material being utilized, varactor diodes can be analyzed in two categories. Gallium arsenide is utilized in high-frequency applications, and silicon is used in low-frequency applications. Additionally, based on their doping profiles, they might be categorized into different classes. Hyperabrupt junctions provide significant

variations in capacitance for a relatively small voltage modification, while linearly graded and abrupt junctions offer less variation of capacitance with changing reverse bias voltage [75].

4.2 Design Procedure

The chosen varactor diode to create the electrically tunable filter is the gallium arsenide flip chip hyper abrupt varactor from MACOM with part number MA46H120. There are multiple reasons for choosing this diode. First of all, the small size of the diode (0.64 mm x 0.32 mm x 0.15 mm) coincides with the purpose of realizing a compact filter. The other reason is that it has a working range that covers all required capacitance values and can be used as a surface mount. Additionally, the Q factor is high and the parasitic capacitance value is low. The features of the varactor diode can be found in Appendix C.

Once the varactor diode that best suits the requirements has been chosen, the component is investigated further using a straightforward circuit design. Figure 4.2 shows the schematic of the designed circuit. As can be seen from the circuit, a high pass filter configuration is created by connecting the varactor between the input and output ports. Also, the varactor is connected to the supply voltage in reverse bias, based on the theory explained previously. Moreover, a test point is added to the PCB to provide supply voltage externally. Furthermore, RF choke inductances are positioned in the ground lines and DC voltage continuation. The chosen inductance value is 15 nH to isolate the supply and RF circuit. It is important to note that, the impedance value set should be at least ten times that of the circuit impedance in the frequency range where the measurement is intended to be taken. For this study, this value can be considered as 500 Ω. Based on this information, Equation (4.1) is used to calculate the reactance value of the inductor. At the same time, it is important to make sure the inserted inductor can handle the applied bias current.

$$X_L = 2\pi f L \tag{4.1}$$

The input and output of the PCB are connected via SMP connectors, which are employed throughout the thesis and have a broad frequency operating range from DC to 18 GHz. The connection between SMPs and the resonator is provided through coplanar waveguide lines. The width of the RF line is calculated considering that the material to be used is RO4003. It is calculated that there should be an 8 mil broad gap and a 34 mil wide RF line for a 20 mil card thickness. DC block capacitances are also placed on the RF line with a value of 100 nF in order to isolate RF AC signal propagation from the DC signal. It is important to make sure that the X_C value is significantly less than the circuit system impedance. Reactance with less than 5 Ω is adequate for this purpose in this design. Equation (4.2) is used to compute reactance. A voltage rating that can withstand the applied voltage is also taken into consideration when selecting the capacitance, and attention is given to ensure that the equivalent series resistance (ESR) value is modest to minimize losses.

$$X_C = \frac{1}{2\pi f C} \tag{4.2}$$

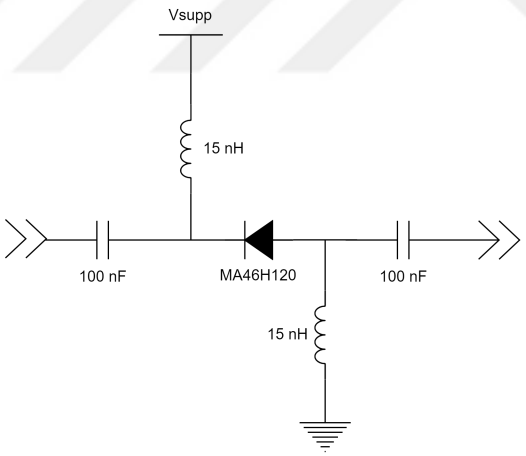


Figure 4.2: Circuit Design with Varactor Diode

The Mentor Pads application is used to sketch the layout of the designed fundamental circuit before it is manufactured. An image illustrating the final outcome is displayed in Figure 4.3.

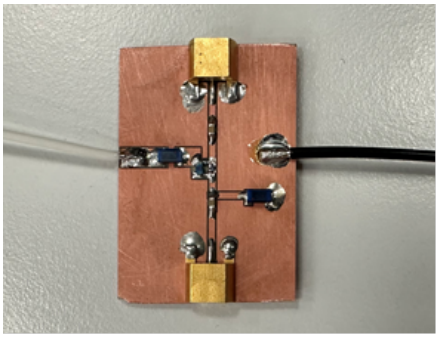


Figure 4.3: Manufacturing Outcome of Circuit Design with Varactor

The performance function of the varactor is obtained from the typical performance curve given in the datasheet using the curve fitting toolbox of MATLAB. The agreement of the datasheet and function is demonstrated in Figure 4.4. The resulting function of varactor capacitance C_{var} is as in Equation (4.3).

$$C_{var} = \frac{(0.0902 \times V^3 + 0.4361 \times V^2 - 5.0692 \times V + 12.4571)}{(V^3 - 6.0024 \times V^2 + 10.5163 \times V + 3.2684)} \tag{4.3}$$

Then, the change in the characteristics of the designed filter is examined with the help of this function, depending on the changing voltage values.

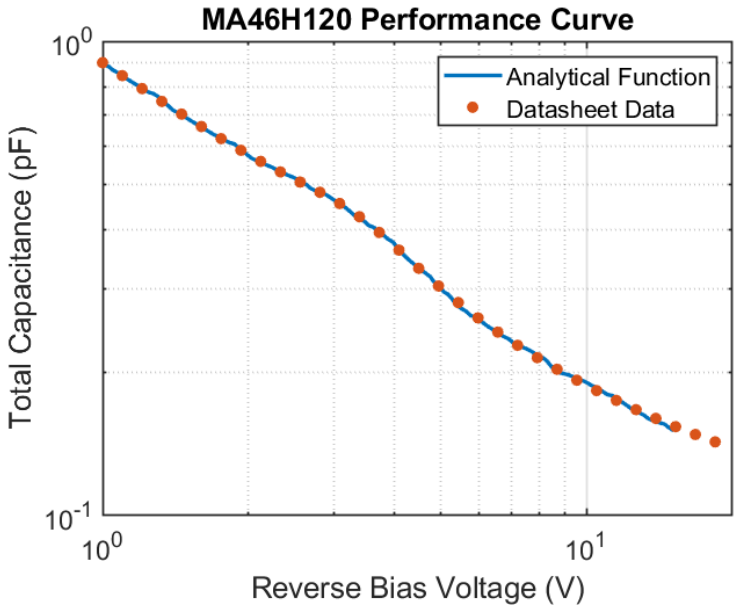


Figure 4.4: MA46H120 Performance Curve

Figure 4.5 illustrates how the S_{21} parameter of the circuit changes in response to variations in voltage and, consequently, in the capacitance of the varactor diode. The capacitance effect and the low-frequency high pass characteristic both diminish with increasing voltage, as predicted.

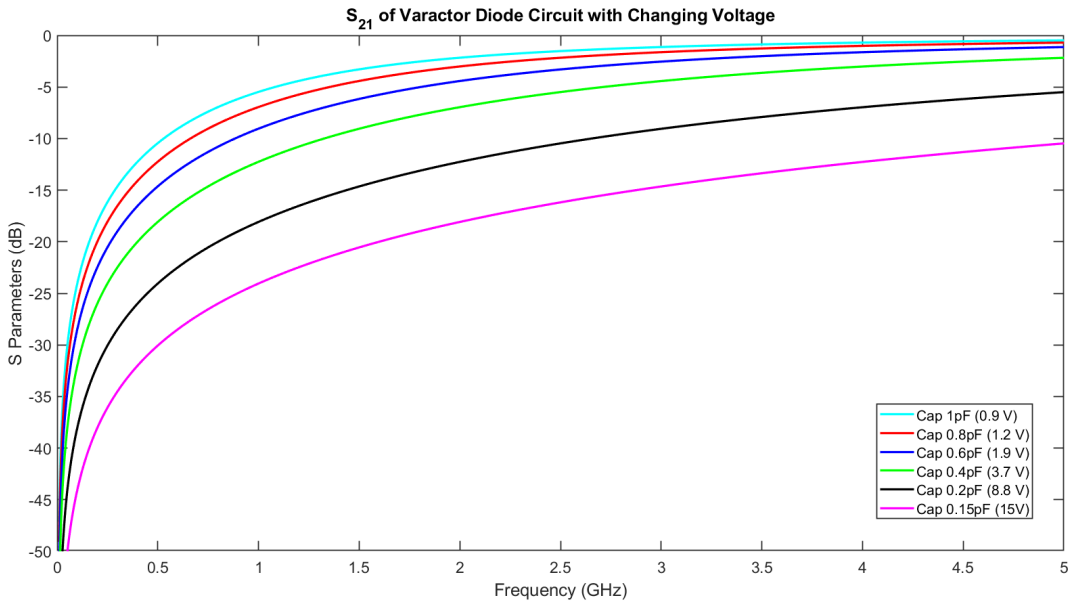


Figure 4.5: S Parameter of Circuit Design with Varactor

After this varactor diode is selected and its functionality is empirically confirmed, the layout of the designed BPF is modified to accommodate them. As a result of this modification, pads are added between the resonators to provide the required bias voltage to the varactor for tuning. During this change, the symmetry in the filter is preserved. The filter layout is modified so that the MA46H120s are placed back to back. In this way, linearity is improved and the DC bias point is isolated from the rest of the filter [76]. Additionally, parasitic effects introduced by the biasing pad are prevented by the back-to-back topology [77]. To give the required voltage, these pads are then connected to other pads that are installed around the filter. Gold ribbon wire bonds, 10 mils wide, were used to provide the connection. The coupling capacitances between the co-planar waveguide and the resonators at the input and output of the filter also served as DC block capacitances, protecting the VNA against possible damage. The mentioned updated layout is shown in Figure 4.6 including the placement of wire bonds and varactors. In order to minimize the size of the layout and

preserve the filter characteristics, ground capacitances, and coupling capacitances are still used as lumped components in addition to the distributed ones. Furthermore, the reverse bias voltages are determined to be the same for the varactors forming the 1st and 2nd inter-resonator coupling, and for the varactors forming the 3rd and 4th inter-resonator coupling. This is a result of the symmetrical component values of the filter from the start of the design process. Thus, it is planned to use two separate voltages to tune the filter. While V_1 determines the higher cutoff frequency, V_2 determines the lower cutoff frequency.

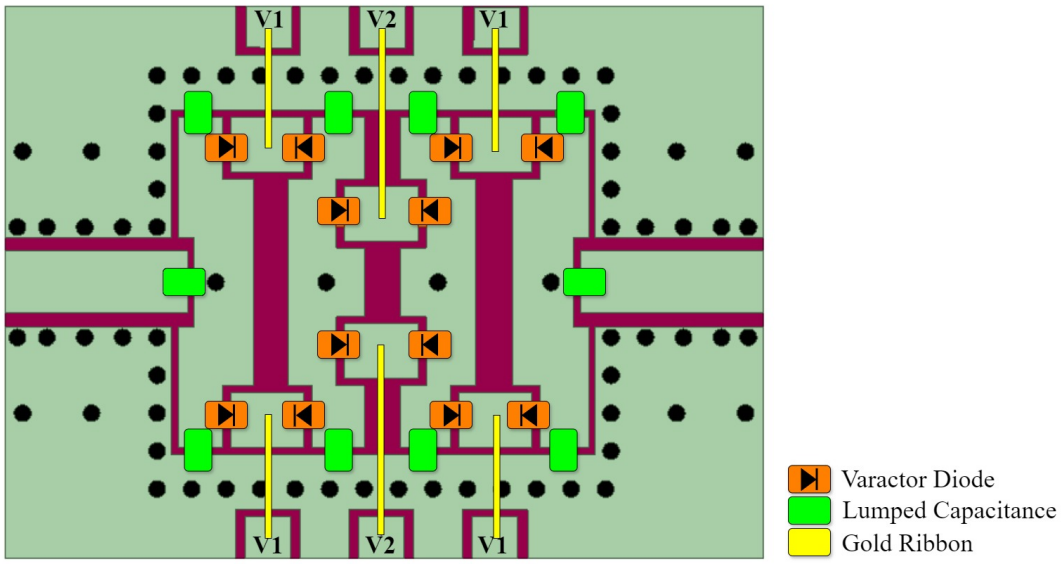


Figure 4.6: Second Version of BPF

When the capacitance contributing to the lower cutoff is set to 0.5 pF and the capacitance impacting the upper cutoff to 0.15 pF, the filter characteristic shown in Figure 4.7 is obtained. These values are achieved by setting the diode voltages V_1 and V_2 to 14 and 2.6 V, respectively. Moreover, to provide DC and RF isolation, an additional 15 nH RF choke inductors are added to the bias path. Examining the S parameters in Figure 4.7 reveals that the goal of S_{11} being below -10 dB is accomplished. Similarly, the filter has an IL that is less than 1 dB. Additionally, more than 25 dB suppression is achieved at out-of-band frequencies higher than 7 GHz and lower than 3 GHz.

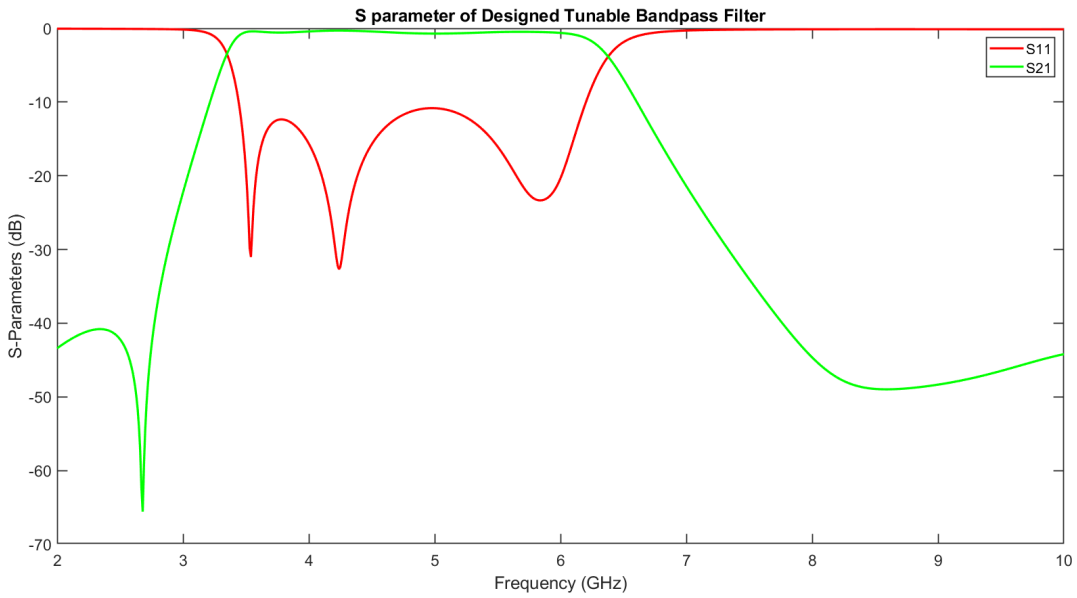


Figure 4.7: S Parameter of Tunable BPF

4.3 Circuit Representation

The circuit model previously developed in Figure 3.25 is modified so that it can be compatible with the adjustable filter. The bias plates of the varactors cause the addition of C_{VS} and C_{VP} capacitances to the circuit as shown in Figure 4.8. The capacitance between the bias plate and the resonator is represented by C_{VS}, whereas the capacitance between the bias plate and the ground is indicated by C_{VP}. Since two plates are inserted between each resonator in the layout, the varactor plate capacitances are connected to the schematic as two structures in parallel. Additionally, the values between the first and second resonators and the values between the third and fourth resonators are indicated as equal because the filter has a symmetrical design. Moreover, the lumped series capacitors from the previous version that were utilized to modify the cutoff frequencies are eliminated. Therefore, only distributed capacitance values are remaining to calculate C_S values between the consecutive resonators.

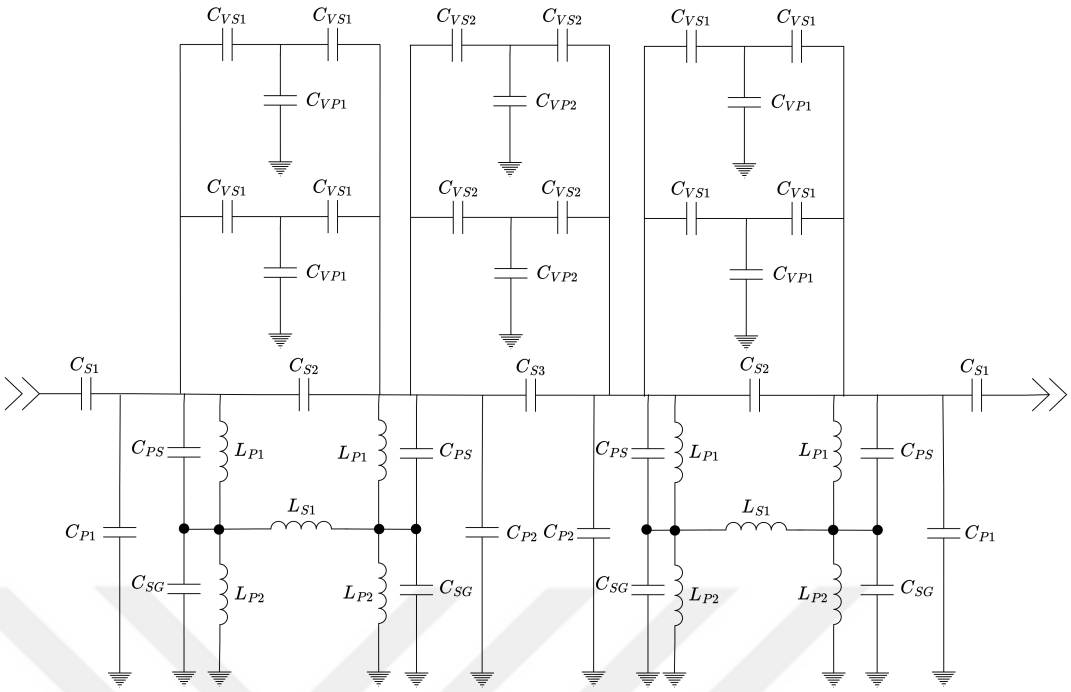


Figure 4.8: Circuit Representation of Tunable Filter

The physical equivalents of the newly added circuit elements in the tunable filter are shown in Figure 4.9. Some structures in the filter design are hidden for ease of display.

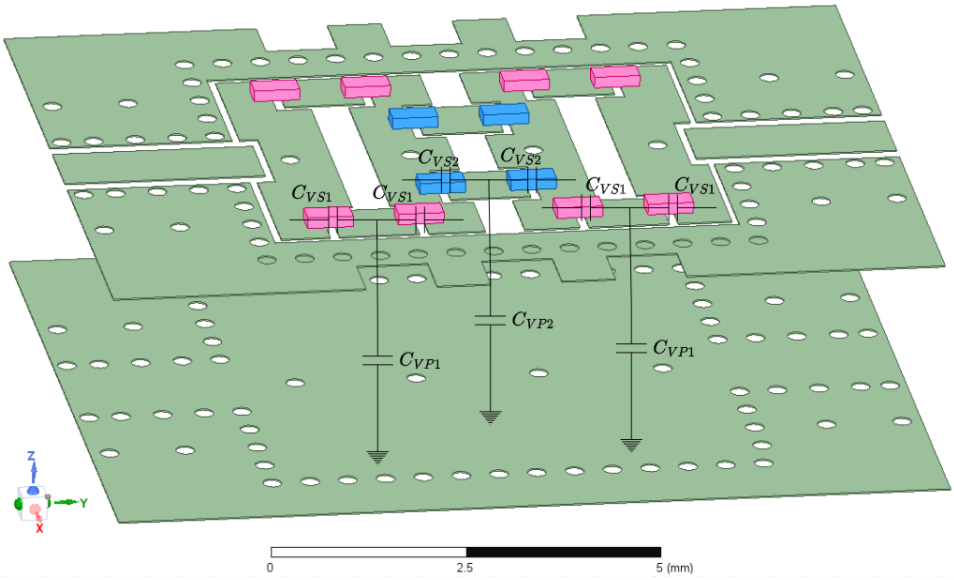


Figure 4.9: Physical Equivalents of the Added Circuit Elements in the Filter Design

The structure of the new short circuit line illustrated in Figure 4.10 is taken into consideration while recalculating the inductance values L_P, and L_S.

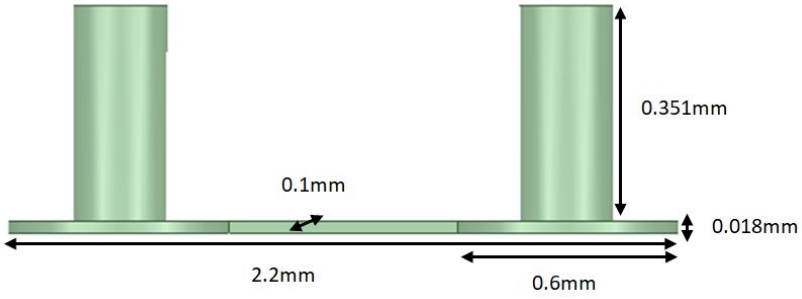


Figure 4.10: Short Circuit Line Structure of Tunable BPF

The inductance of through via is the same because the card thickness does not change. By proportioning this inductance value of 1.565 nH in accordance with the layer in the stack up where the short circuit line is positioned, the L_{P1} and L_{P2} values are determined as 0.2103 nH and 1.3547 nH.

Afterward, the Q3D analysis of the short circuit line structure is used to determine the inductance value. A frequency-dependent change in inductance is seen in Figure 4.11. This simulation result of 1.078 nH is used to determine the L_{S1} value as 0.6574 nH by subtracting the effect of L_{P1}.

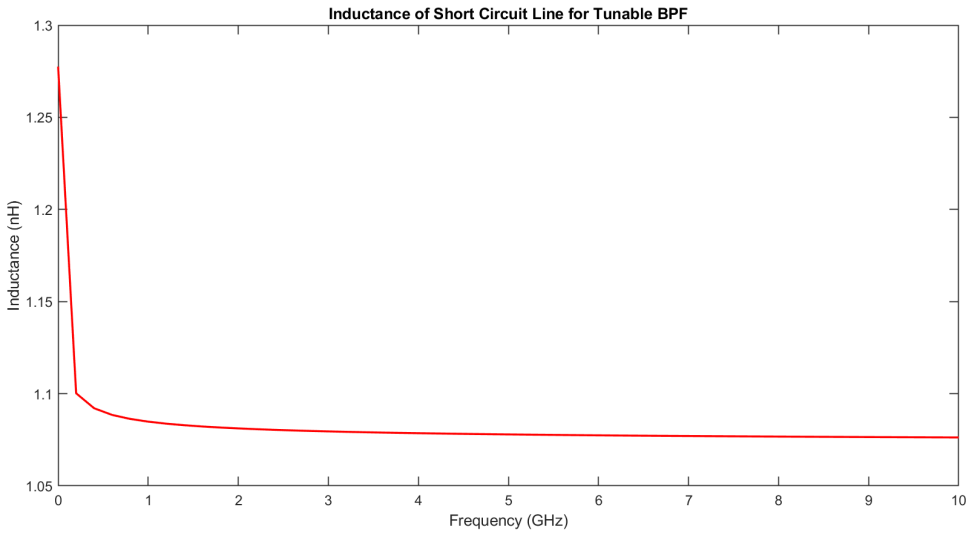


Figure 4.11: Inductance of Short Circuit Line Used in Designed Tunable Filter

After determining the inductance values to be used in the circuit, studies are carried out for capacitance. As only the value resulting from the distributed capacitance remained, the capacitance for C_{S2} and C_{S3} lowered to an almost insignificant level. The filter characteristics are determined by the capacitances that are supplied by the varactor diodes themselves which are C_{VS1} and C_{VS2}. Furthermore, the capacitance value formed between the varactor bias plates and the ground is identified using Q3D simulations. In the circuit diagram, these values are designated as C_{VP1} and C_{VP2}. Moreover, the C_{PS} value increased and the C_{SG} value dropped as anticipated since the short circuit line is at a higher layer than the prior version of the designed filter. Following the determination of other parameters, the values of C_{P1} and C_{P2} are adjusted, and their values are slightly reduced as expected. The revised layout confirms the decrease in capacitance because the resonators are smaller. Table 4.1 provides a summary of all used values. When the schematic is adjusted using these values, the frequency response in Figure 4.12 is observed. There is a high degree of consistency between the schematic and the 3D model simulation results. However, both the lower and higher band cutoff frequencies are found to have a small amount of inaccuracy.

Table 4.1: Resultant Values of Circuit Components for Tunable BPF

Component	Value	Component	Value
C_{S1}	0.98 pF	C_{VS1}	0.20 pF
C_{S2}	0.02 pF	C_{VS2}	0.51 pF
C_{S3}	0.01 pF	C_{VP1}	0.09 pF
C_{P1}	0.50 pF	C_{VP2}	0.03 pF
C_{P2}	0.62 pF	L_{P1}	0.21 nH
C_{PS}	0.13 pF	L_{P2}	1.355 nH
C_{SG}	0.06 pF	L_{S1}	0.657 nH

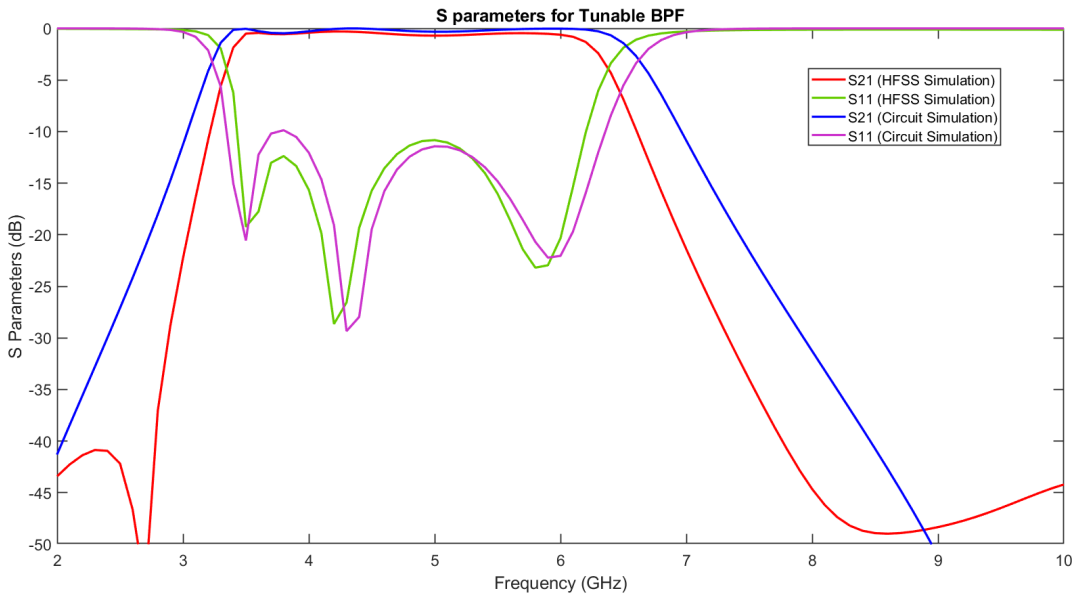


Figure 4.12: Simulation and Measurement Results of Tunable BPF

4.4 Manufacturing and Measurement Results

The stack-up of the designed updated tunable filter is shown in Figure 4.13. The figure shows that the prepreg and core are made of the same materials and have the same thicknesses as the previous version of the filter. As a result, the manufacturing tolerances and modification of the copper layers created a minimal change in the total board thickness. The short circuit line is located in a higher layer with respect to the first design.

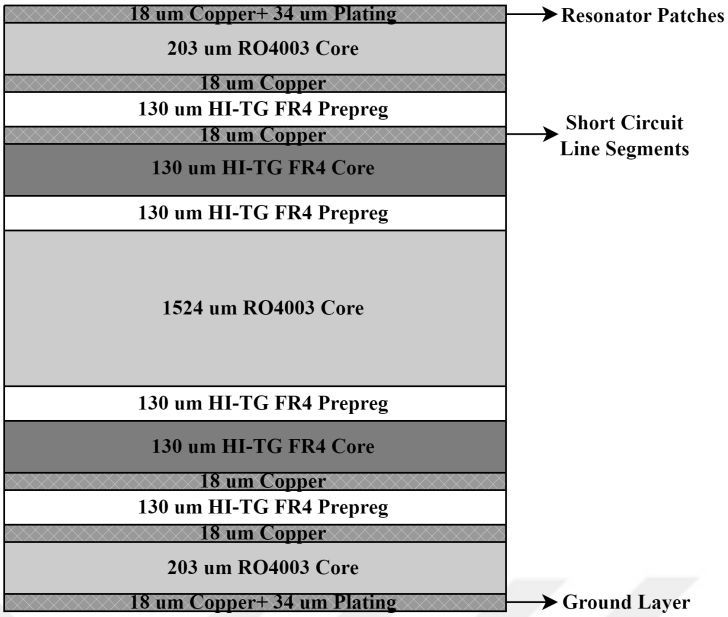


Figure 4.13: Stackup of BPF v2

The top layer of the layout of the reconfigurable filter is depicted in Figure 4.14. The planes that appear gray are copper, while the layer that appears yellow is the solder mask layer.

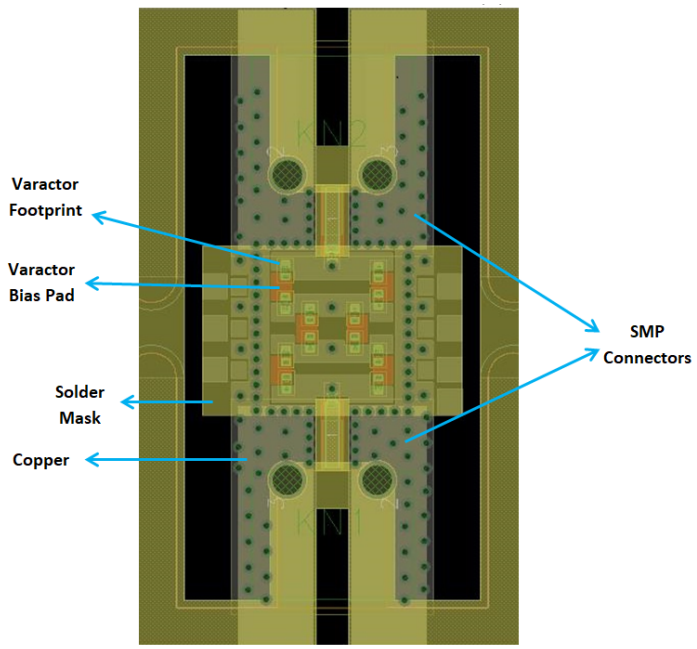


Figure 4.14: Layout of BPF v2

The developed reconfigurable filter has 12 pieces of MA46H120, 0.9 pF coupling capacitances, and 0.1 pF ground capacitances soldered to it. The filter is prepared for measurement once each bias pad is connected to the external interface using a gold ribbon. In Figure 4.15, the filter that is obtained from the investigation is demonstrated.

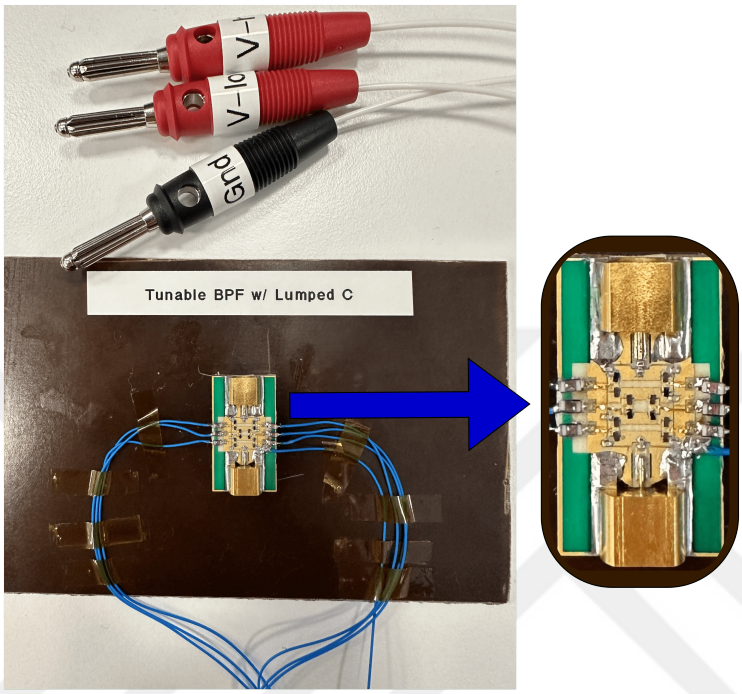


Figure 4.15: Manufacturing Result of Tunable BPF with Lumped C

While measuring the filter, the required voltages are supplied to the circuit by using the power supply together with the VNA used in the previous filter tests. The utilized measurement setup can be seen in Figure 4.16. Measurement results are obtained as shown in Figure 4.17. Because of nonidealities in real life, in-band IL is higher than in the simulation, while RL is less. Additionally, a shift to the right is observed at the higher and lower cutoff positions. Research on the factors that may mitigate these alterations is still ongoing.

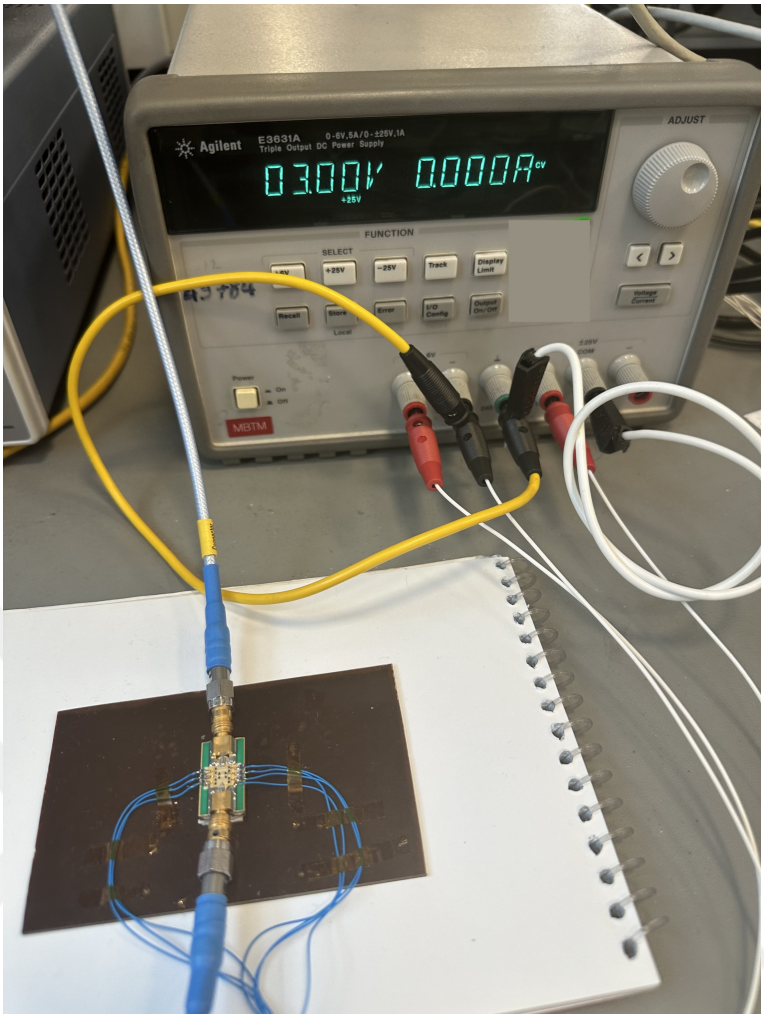


Figure 4.16: Measurement Setup for Tunable Filters

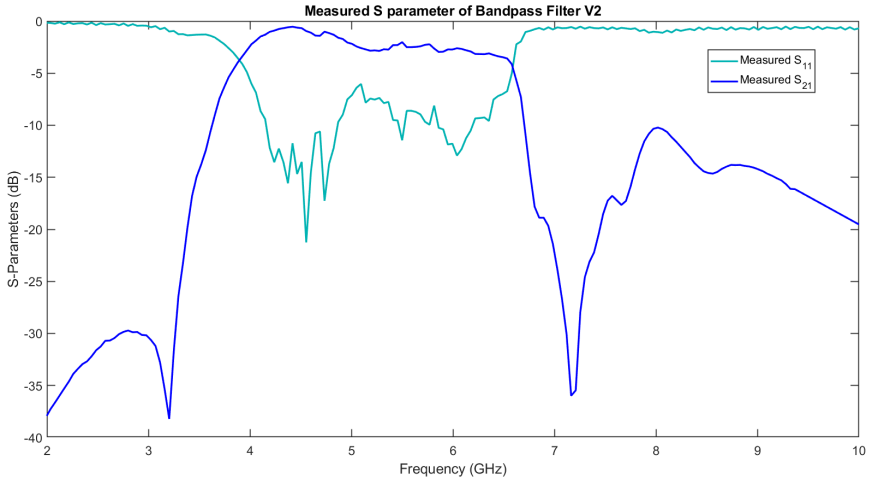


Figure 4.17: Measurement Result of Tunable BPF with Lumped Capacitances

4.5 Optimized Tunable SIW Bandpass Filter with Distributed Ground Capacitances

Although the tunable filter, whose design is described and tested in earlier sections of Chapter 4, has advantages such as being compact, being voltage tuned, and having good selectivity, it also has some improvable features. Reducing the number of elements in the filter structure can be given as the first example. Another thing that can be developed is to ensure that the ground capacitors with optimal values can be used. Furthermore, the capacitance tolerances are higher in percentage terms since the capacitors are employed at very low capacitance values. Increased variations in capacitance have a greater impact on the filter response. Alternatively, a solution with less variance can be relied on. As a common solution for all these disadvantages, it is aimed to convert lumped capacitors into distributed forms. This reduces the number of lumped elements in the circuit and compensates for the cost increase because of the varactor diodes. Only the capacitors that provide external coupling remain as lumped circuit elements. Additionally, the capacitance values realized with parallel plates can be selected as the optimum size, as different EM simulations can optimize the plate size. These plates have far less manufacturing tolerances than the lumped element.

The ground capacitances are formed by plates whose widths are determined as a constant 0.5 mm. Moreover, the length of 0.8 mm from the ground via to the bottom of the resonator is defined by default for all plates. Afterward, a manual grid search is performed to find appropriate lengths to add to this default value. In other words, combinations of C_{P1} and C_{P2} capacitance plates of various lengths are systematically tested. Figure 4.18 illustrates the grid that is utilized for the investigation. Grid selection is done based on the full wave 3D model analysis in the trials. The effect of the capacitance created by the selected length on the S_{11} characteristic is examined for multiple BWs with 0.1 mm resolution. The choice of which way to go on the grid depends on whether or not the length adjustment results in an improvement. First, the length combinations at the four corner points and the midpoint of the largest solution set are tried. This process is then adaptively repeated for the interval that gives good results. For the C_{P1} plate, the most optimal outcome is found to be 1.2 mm, while for the C_{P2} plate, it is 0 mm.

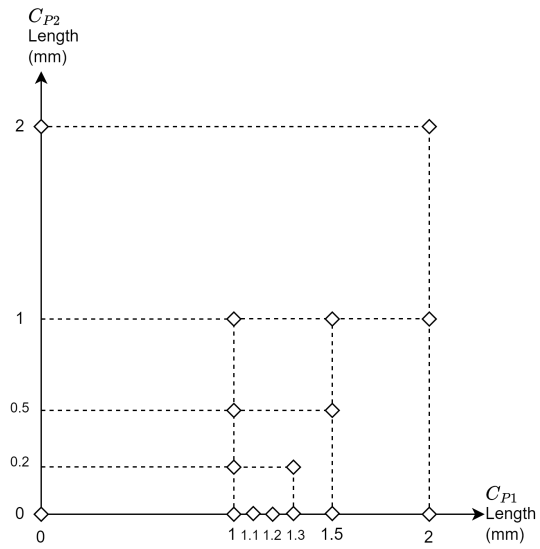
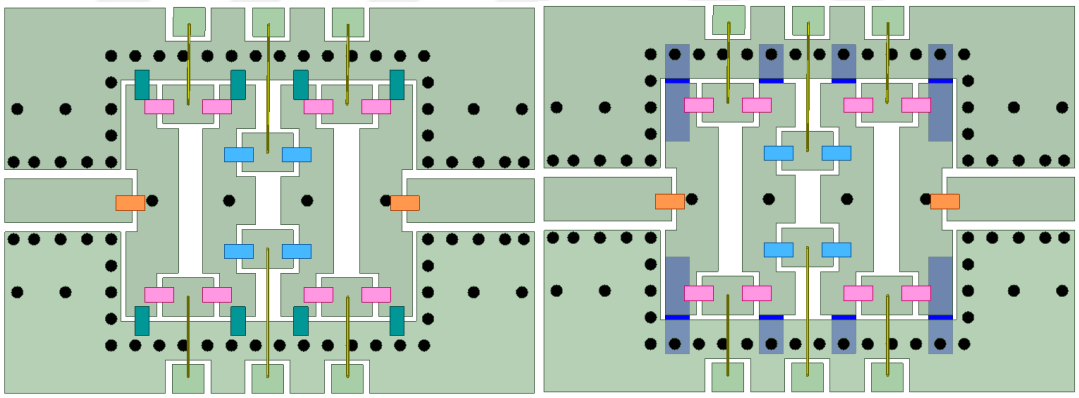


Figure 4.18: Grid Search Map for the Ground Capacitance Combinations

Figure 4.19 shows the initial state of the tunable filter with lumped capacity and the layout that formed after the size of the distributed plates is determined. The top copper layer is made transparent and the plates placed on the bottom layer are shown.



(a) Lumped Ground Capacitances (b) Distributed Ground Capacitances

Figure 4.19: Tunable BPF Top View

HFSS simulation is carried out for the determined optimum C_P plate lengths by varying varactor bias voltages V_1 between 4V - 13V and V_2 between 3V - 4V. Given that all BWs are taken into account, -11.53 dB is found to be the maximum return loss. When the voltages of V_1 and V_2 are both 4V, the BW is the narrowest. Accordingly,

when the V_1 value is 13 V and the V_2 value is 3 V, the BW of the designed filter is the widest. The filter characteristics obtained as a result of these limit voltage values are shown in Figure 4.20.

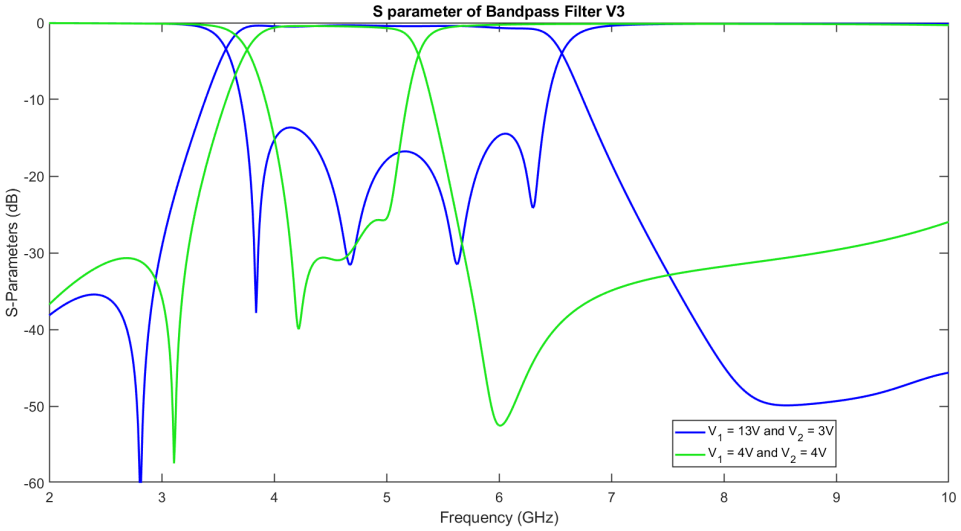


Figure 4.20: Simulation Results of Tunable BPF with Distributed Capacitances for Limit Voltage Values

The higher cutoff frequency shifts to the right as V_1 voltage increases. It is achievable to adjust the higher cutoff frequency from 5.24 GHz to 6.52 GHz as in Figure 4.21.

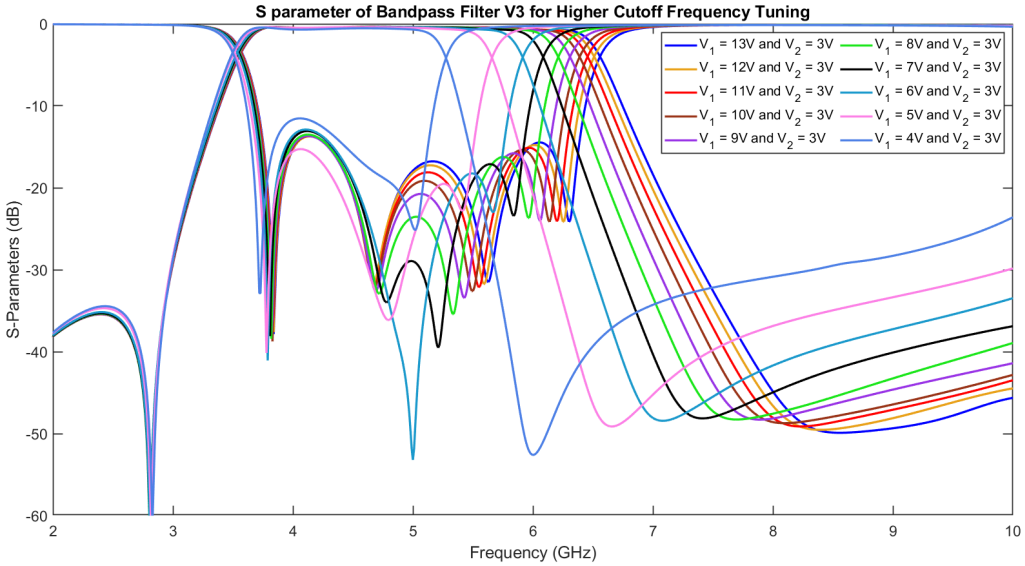


Figure 4.21: Simulation Results of Tunable BPF with Distributed Capacitances for Higher Cutoff Tuning

The lower cutoff moves to the left and BW enlarges as the V_2 voltage decreases. In scenarios when the S_{11} value remains consistently below -10 dB for the passband, it is possible to adjust the lower cutoff frequency to a range of 3.85 GHz to 3.5 GHz as shown in Figure 4.22.

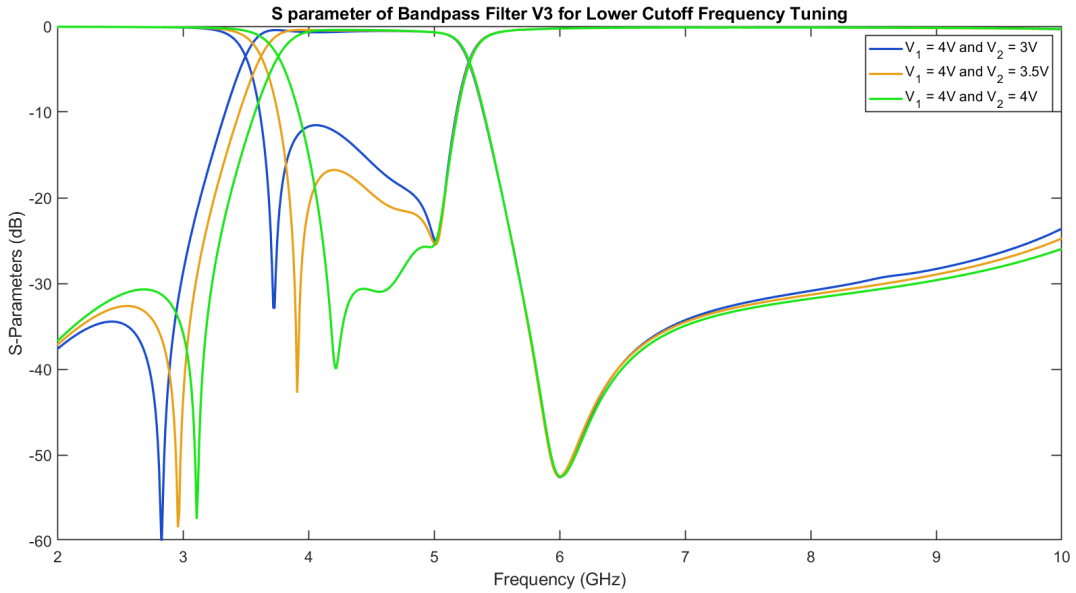


Figure 4.22: Simulation Results of Tunable BPF with Distributed Capacitances for Lower Cutoff Tuning

The circuit representation in Figure 4.8 is also valid for this configuration. The difference from the previous version is that only distributed values are used when calculating C_P values. The amount of capacitance that corresponds to the plate added to the filter design is computed using the calculation in Equation (4.4). It is found that the capacitance introduced by the parallel plate is 0.093 pF for 0.5 mm $\times$ 1.2 mm area plate. The overall utilized component values are shown in Table 4.2.

$$C = \frac{\epsilon_0 \epsilon_r A}{d} \tag{4.4}$$

Table 4.2: Resultant Values of Circuit Components for Tunable BPF with Distributed Capacitances

Component	Value	Component	Value
C_{S1}	0.98 pF	C_{VS1}	0.20 pF
C_{S2}	0.02 pF	C_{VS2}	0.51 pF
C_{S3}	0.01 pF	C_{VP1}	0.09 pF
C_{P1}	0.44 pF	C_{VP2}	0.03 pF
C_{P2}	0.54 pF	L_{P1}	0.21 nH
C_{PS}	0.13 pF	L_{P2}	1.355 nH
C_{SG}	0.06 pF	L_{S1}	0.657 nH

Moreover, the frequency response acquired with recently introduced parallel distributed ground capacitances and series lumped capacitance values used in the previous version of BPF (Figure 4.12) is displayed in Figure 4.23.

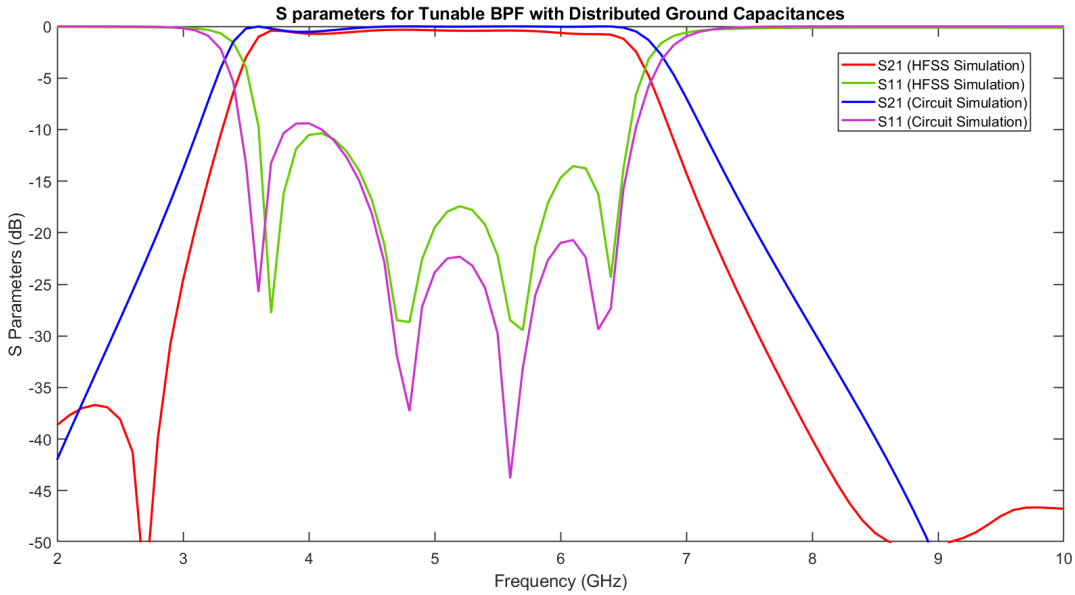


Figure 4.23: Simulation and Measurement Results of Tunable BPF with Distributed Capacitances

Two significant conclusions can be obtained from Figure 4.23. The first one is that the contribution of distributed capacitance to the filter characteristic is revealed through simulation. Giving more precise ground capacity values enables the RZs in S_{11} to

be positioned more effectively within the pass band. Another conclusion is that the consistency between the circuit and the simulation continued to be maintained. There are minimal differences in cutoff frequencies.

4.6 Manufacturing and Measurement Results

The stackup of the designed updated tunable filter is shown in Figure 4.24. The stackup is the same as the adjustable BPF stackup shown in Figure 4.13. The layout now includes a design specifically for ground-capacity plates in the second layer. The plates that form the distributed ground capacitances are positioned closest to the upper layer. In this way, the distance between the two conductors is reduced and a larger capacitance is obtained with a smaller plate size.

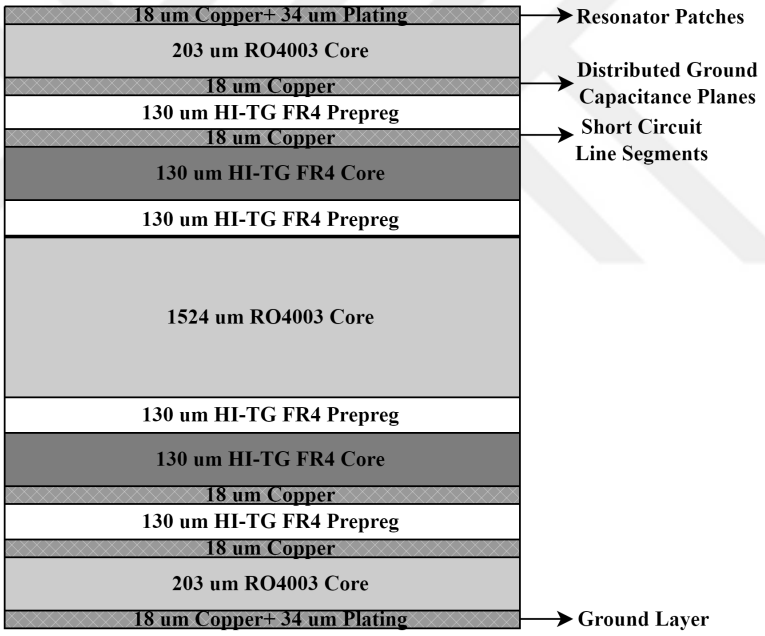


Figure 4.24: Stackup of Tunable BPF with Distributed Capacitances

The final version of the layout design is shown in Figure 4.25. The configuration includes the through line, versions of the tunable filter with lumped capacitances, and distributed ground capacitances. Moreover, PCB breakaway tabs are added to the design so that three types of cards can be separated into smaller sections and independently researched.

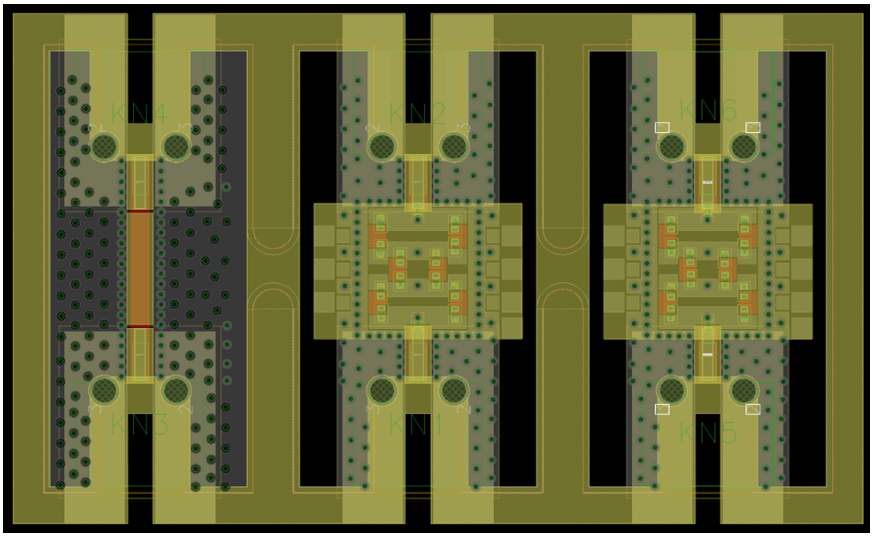


Figure 4.25: Final Version of Layout

The intermediate layer layout drawing with size-optimized capacitance plates is displayed in Figure 4.26.

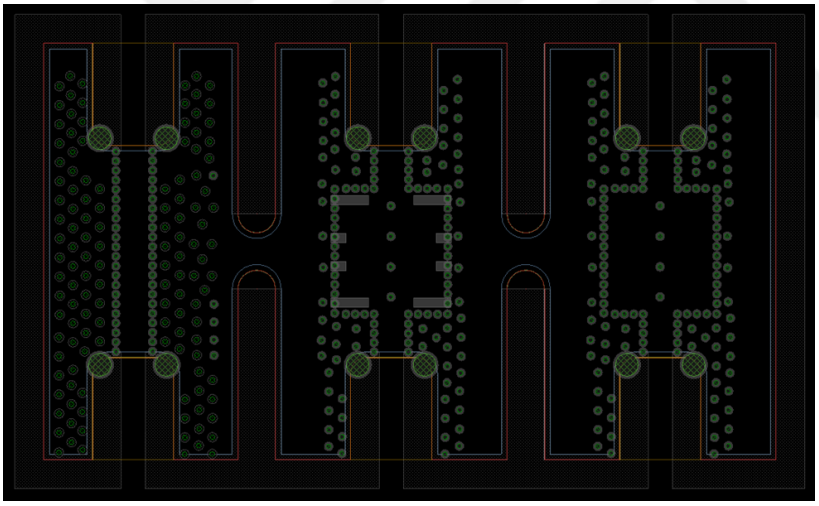


Figure 4.26: Intermediate Layer of Layout

In Figure 4.27, the filter that is obtained from the investigation is demonstrated.

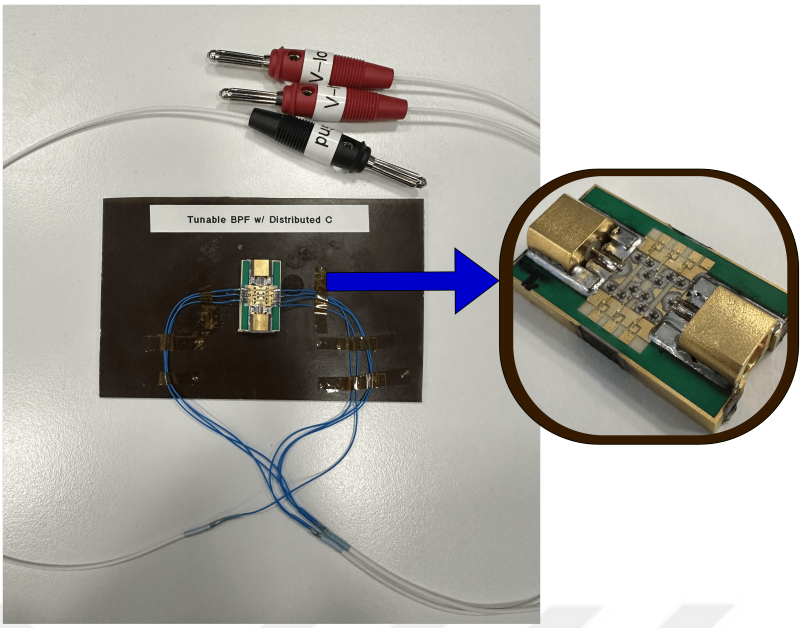


Figure 4.27: Manufacturing Result of Tunable BPF with Distributed C

While measuring the filter, the same setup shown in Figure 4.16 is used. Figure 4.28 shows the measurement data obtained by changing the V_2 voltage value between 3 V and 4 V with 0.5 V intervals in order to tune the lower cutoff frequency. It is observed that the lower cutoff can be controlled as intended. Likewise, measurement data are taken by decreasing the V_1 value from 13 V to 4 V at 1 V intervals. As a result, the higher cutoff frequency of the filter can be controlled. Nevertheless, in both figures, IL and RL are different than expected due to the losses brought to the system by the materials used in real life, tolerances occurring throughout the manufacturing processes, and other non-idealities.

There may be some reasons for selecting the tunable filter even though it has a higher IL than the filter with a fixed frequency response. When a highly accurate filter is required for high-performance radar or sensitive communication channels, the tunable option may be preferred. The ability to adjust the lower and upper cutoff frequencies independently is an element that increases precise tuning capability. Another reason may be to prevent specific interferences to the receiver during operation. However, this filter directly increases the noise figure when it is used before LNA. For this reason, the designer must make a choice between being tunable or having lower IL, according to the system specifications.

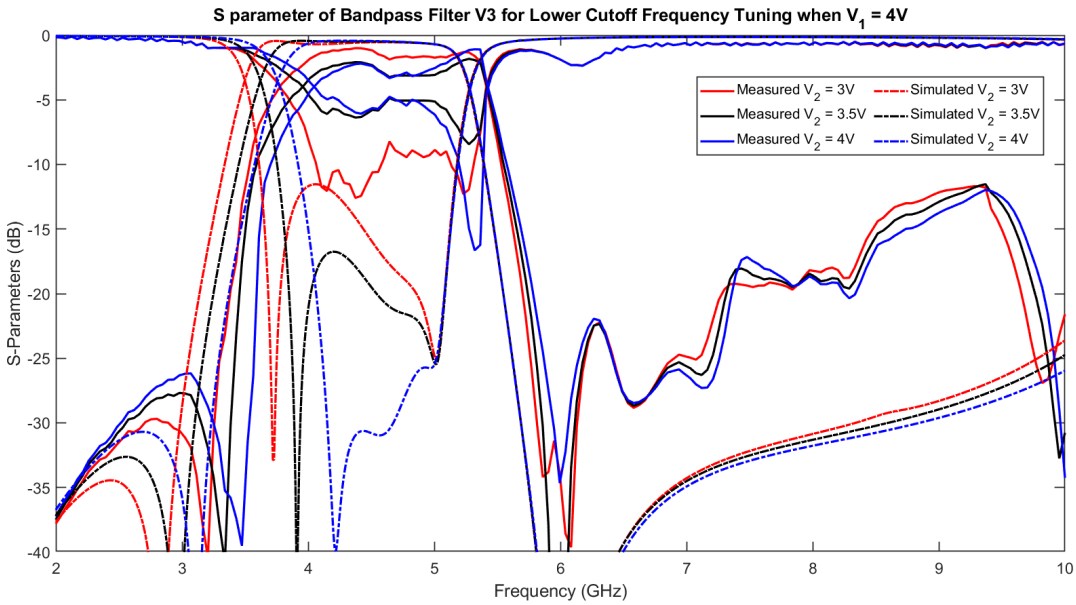


Figure 4.28: Frequency Response of Tunable BPF with Distributed Capacitances for Lower Cutoff Tuning

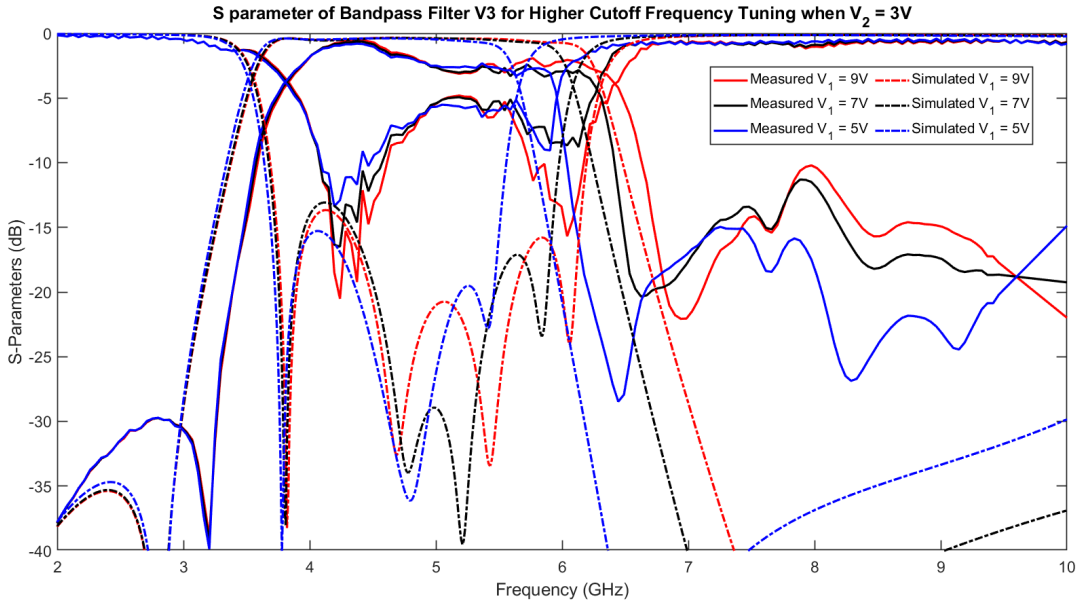


Figure 4.29: Frequency Response of Tunable BPF with Distributed Capacitances for Higher Cutoff Tuning

CHAPTER 5

CONCLUSIONS

This thesis introduces a compact wideband bandpass filter designed to function within the S/C Band frequency range (3.5 - 6 GHz). The filter boasts several beneficial characteristics, including high out-of-band rejection, low IL, and high return loss. It is ideal for applications in satellite communication, channelized receivers for RF tasks, front-end units, as well as measurement and test equipment. Filters are essential for excluding unwanted signals from a particular RF channel in a broad frequency spectrum, thereby enabling effective signal processing. The required features of the filter are specified based on the configuration of the RF strip into which it is integrated.

Initially, various techniques from the literature are reviewed to meet the specified requirements. A hybrid approach is selected, combining surface-mounted bulk capacitors with the substrate-integrated waveguide technique to design the filter. This approach aims to minimize the size of the filter while enhancing its shielding effectiveness. The first step in the filter design involves constructing the basic resonator structure. A detailed analysis of the factors affecting the performance of the resonator, such as via diameter, conductor plane width, and dielectric thickness, is performed. Subsequently, both analytical and computational methods are employed to explore the mechanisms of dual coupling. The research leads to the development of a fourth-order bandpass filter design. The final manufactured product measures are 0.088λ x 0.095λ, excluding the connectors. Measurements confirm that the desired out-of-band suppression is achieved with an IL of less than 2 dB, as predicted by simulations. Additionally, suppression at frequencies adjacent to the band exceeds 30 dB, and the minimum in-band return loss is 12 dB for the designed filter. A code that could optimize the filter is also suggested. The PSO algorithm implemented with MATLAB

provides considerably faster and equally optimal determination of the ground capacitance values employed in the design. Next, an electrically tunable version of the filter is developed using varactor diodes, allowing the filter to adapt to changing conditions without manual intervention. Step-by-step modeling and design procedures are provided. Wire bond technology is utilized to supply the necessary bias voltage for tuning the varactor. The manufactured filter is tested using a vector network analyzer and voltage supply, confirming that the lower and upper cutoff frequencies can be independently adjusted with two distinct voltages. Moreover, this modification results in minimal enlargement of the filter and negligible power consumption. Circuit representations of the proposed filters are examined at each stage to facilitate and expedite the design process, ensuring compatibility with simulations. Once the tunable filter design is finalized, ground capacitors are transformed into a distributed form to achieve finely tuned capacitance values and reduce the number of elements in the design. An iterative grid search process is used to determine the optimal parallel plate dimensions for the widest band gap. The enhanced filter is manufactured and tested, with measurement data confirming that the filter can be adjusted using voltage as designed. The third study that can be carried out involves using vias rather than wire bond technology to connect the bias voltages to the bias pads in the tunable filter. The manufacturing of the filter becomes easier with this technique. Furthermore, the disadvantage of wire bonds being deformed due to external factors is eliminated.

There are several different studies planned to be conducted in the future to further develop the study. The first of these is the adaptation of the PSO algorithm developed for the filter designed in the study to the tunable version. This improvement can be done for both lumped and distributed cases of ground capacitances. The code can be developed to be a multitarget PSO. In this way, optimized ground capacitance values can be selected to be suitable for more than one band at the same time. The advantage of this is that the computationally difficult process, which normally takes a long time during the design, can be solved in a shorter time with respect to the grid search method. Another improvement can be converting the filter from a connectorized structure to a surface mountable structure. This makes it possible to integrate filters into RF paths in PCB applications, regardless of the stack-up.

To conclude, this work develops a bandpass filter with characteristics appropriate for wideband channelized receivers. Then, a reconfigurable version of the filter is presented. Afterward, it is described how optimization techniques are used to lower the number of circuit components in the filter. Finally, circuit diagrams are improved to make the entire design process more understandable and to shorten simulation time.

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APPENDIX A

PSO ALGORITHM FUNDAMENTALS

In the PSO algorithm, every potential solution to the elements planned to be optimized is a particle. The initial position of particles in the multidimensional search space can be either randomly assigned or user-determined as in Figure A.1 beginning phase. In each iteration, particles move vectorially at a specific velocity to another position as in Figure A.1 middle phase. The outcome that each particle experiences becomes knowledge that all particles are aware of because of their swarm behavior. Therefore, iterative position updates occur according to the previous knowledge in order to yield better outcomes with each iteration (i) as in Figure A.1 final phase [46].

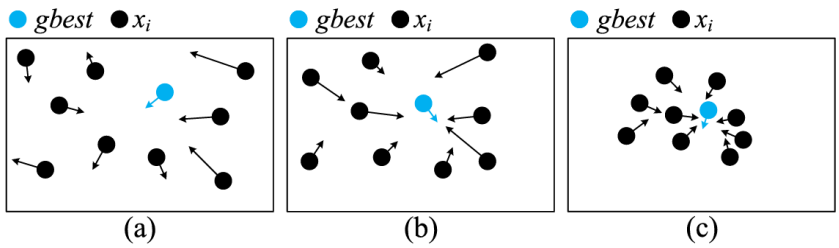


Figure A.1: Three common scenarios for the particles in PSO processes (a) Starting phase (b) Middle phase (c) Final phase [46]

Equation (A.1) describes how velocity (v) updates occur, whereas Equation (A.2) describes position (x) updates. While $pBest$ is the personal best value of the particle it has discovered so far, $gBest$ is the best position that all particles have encountered, that is, the global best. The terms cognitive and social coefficients, respectively, refer to c_1 and c_2. The amount of global and personal feedback that impacts the particle is determined by these coefficients. Inertia weight is denoted by w_{in}. This parameter indicates how much the new velocity is influenced by the prior velocity. The

particle moves more freely and in bigger steps at very high levels of w_in. The PSO algorithm gains stochasticity with the addition of r_1 and r_2 to the equation, which are random decimal numbers between 0 and 1. Until the process is stopped by one of the established criteria, these iterations continue. Achieving a predetermined level of satisfaction or completing the maximum number of instances are two examples of criteria.

$$v_i(t+1) = w_{in} \times v_i(t) + c_1 \times r_1 \times (pBest_i - x_i(t)) + c_2 \times r_2 \times (gBest_i - x_i(t)) \quad \text{(A.1)}$$

$$x_i(t+1) = x_i(t) + v_i(t+1) \quad \text{(A.2)}$$

APPENDIX B

VARACTOR DIODE BASICS

The internal structure and operating principle of the varactor can be summed up as follows if additional in-depth analysis is desired. Three primary layers make up the varactor diode, as shown in Figure B.1. These are the p-type layer with positive charge carriers, the n-type layer with negative carriers, and the depletion region where the two carrier types neutralize each other. The variation in the external voltage applied determines the width of this region.

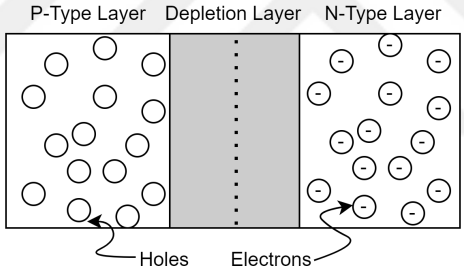


Figure B.1: Varactor Diode Structure

In the case of forward bias (the positively charged side of the voltage connected to the p-layer and the negative side connected to the n-layer), the depletion width decreases or even disappears when applied sufficiently. This situation can be observed from the Figure B.2. In this case, the desired capacitive effect of the varactor cannot be observed. For this reason, varactor is always used in the reverse bias situation as in Figure B.3. In this scenario, charges accumulate at the ends of the diode and the width of the depletion layer increases as the applied voltage increases. As a result, the capacitive impact is diminished. There is an inversely proportional relationship between voltage and capacitance.

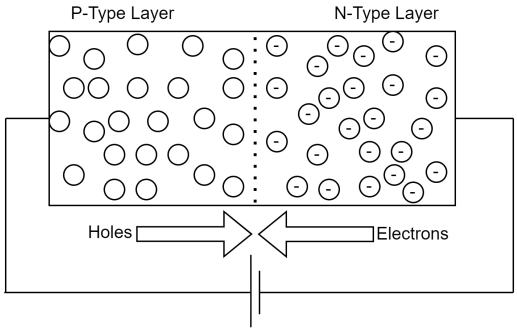


Figure B.2: Forward Biased Varactor

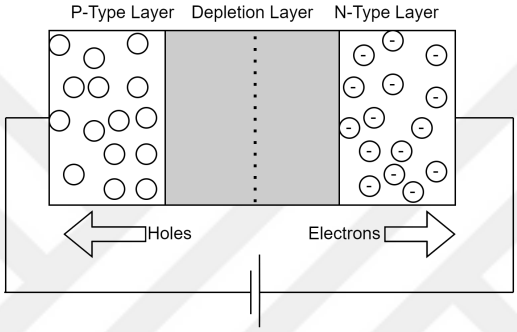


Figure B.3: Reverse Biased Varactor

APPENDIX C

DATASHEET OF VARACTOR DIODE

MA46H120 Series

GaAs Constant Gamma Flip-Chip Varactor Diode Rev. V2

Features

- Constant Gamma for Linear Tuning
- Low Parasitic Capacitance
- High Q
- Silicon Nitride Passivation
- Polyimide Scratch Protection
- Surface Mount Configuration

Description

M/A-COM's MA46H120 series is a gallium arsenide flip chip hyperabrupt varactor diode. These devices are fabricated on OMCVD epitaxial wafers using a process designed for high device uniformity and extremely low parasitics. The MA46H120 diodes are fully passivated with silicon nitride and have an additional layer of polyimide for scratch protection. The protective coatings prevent damage to the junction during automated or manual handling. The flip chip configuration is suitable for pick and place insertion.

Ordering Information

Part Number	Package
MA46H120-W	Whole Wafer
MA46H120	Gel Pack
MAVR-000120-12030W	Waffle Pack

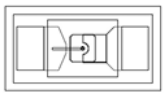
Absolute Maximum Ratings [1,2]

Operating Temperature	-40°C to +125°C
Storage Temperature	-65°C to +150°C
Power Dissipation	100 mW
Mounting Temperature	+235°C for 10 seconds

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. M/A-COM does not recommend sustained operation near these survivability limits.

Chip Layout

Front View (Circuit Side)

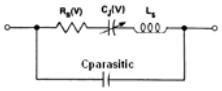


Back View (Operator Side)



Schematic

FLIPCHIP TUNING VARACTOR EQUIVALENT CIRCUIT



Electrical Specifications @ T_A = +25 °C

Breakdown Voltage @ I_R = 10μA, V_R = 20 V Minimum
Reverse Leakage Current @ V_R =14V, I_R = 100 nA Maximum

	C_T (pF) f=1MHz, V_R=0V			C_T (pF) f=1MHz, V_R=4V			C_T (pF) f=1MHz, V_R=10V			Q Factor f=50MHz, V_R=4V			Gamma V_R=2-12V		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
MA46H120		1.1		0.30		0.40	0.14		0.20	3000			0.9		1.1

* Specifications are subject to change without prior notification

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